MIPI CSI-2 Video Output Board

[SVO-03-MIPI]

Hardware Specification

Rev.1.0

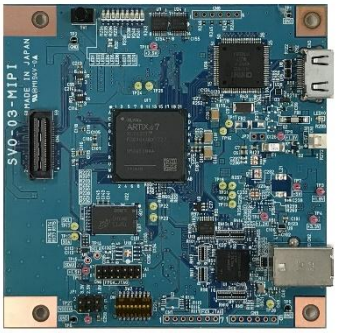
NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	2018/05/02	New File（Equivalent to Japanese version 1.1）	S.Usuba

Index

1. Outline



This document is a hardware specification of the board "SVO-03-MIPI" to convert the video signal from USB 3.0 to the MIPI CSI-2 signal.

The specifications for this book may be changed without prior notice. It also includes descriptions of the features that are not implemented in the product.

1.1. SVO-03-MIPI functions

Video files on computers-> MIPI CSI-2 video signal Conversion

HDMI Signal-> MIPI CSI-2 video signal conversion (optional function)

1.2. Specifications (USB Mode)

Power : USB Bus Supply (External Power Input Applicable) / +5V 0.7A typ.

Output standards : MIPI CSI-2 Video Signal （1 - 4 lane）

Data rate per lane : max. 1Gbps

Effective pixel data Rate : max. 2.4Gbps

MIPI Clock Rate: 50 - 500 MHz (100Mbps – 1000 Mbps)

Output Resolution: max. 4093 x 4093 pixel

Output Pixel Format : YUV4:2:2, Raw10, Raw12, Raw20, RGB24

Input : USB3.0 Connector

Input Resolution, Frame Rate, Pixel Format : Identical to output [1]

[1] If the input format is AVI format, the pixel format on the file supports YUV or RGB24 (DIB).

2. USB Mode operation details

This chapter describes USB mode (USB input, MIPI output).

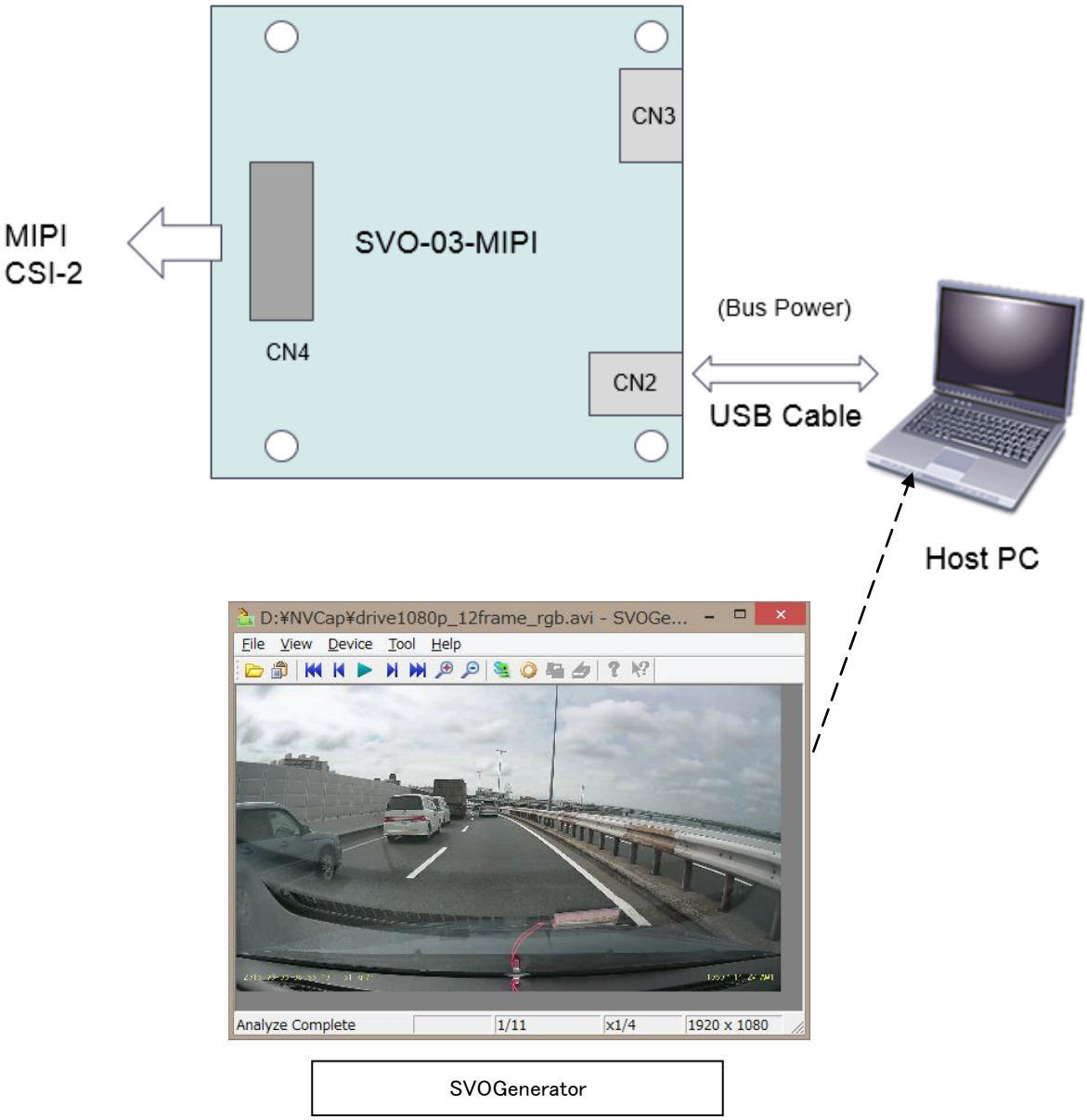
2.1. Main Functions and Features of USB Mode

- Converts an uncompressed avi file or frm file stored on a PC to a MIPI CSI-2 video signal and outputs it.
- We use Meticom's MIPI D-PHY-compliant bridge IC.
- Because the transfer is uncompressed, it does not impair the image quality of the camera and is ideal for evaluation testing and algorithm development.
- Compatible with Windows OS.
- A dedicated video output software (SVOGenerator) is included in the accompanying CD.
- The high-speed transmission of USB 3.0 allows uncompressed video data to be captured up to 3.2 Gbps (theoretical values).
- The target connection side is completely pin-compatible with our existing SVM-MIPI board, so you can immediately

connect your target on the same board.

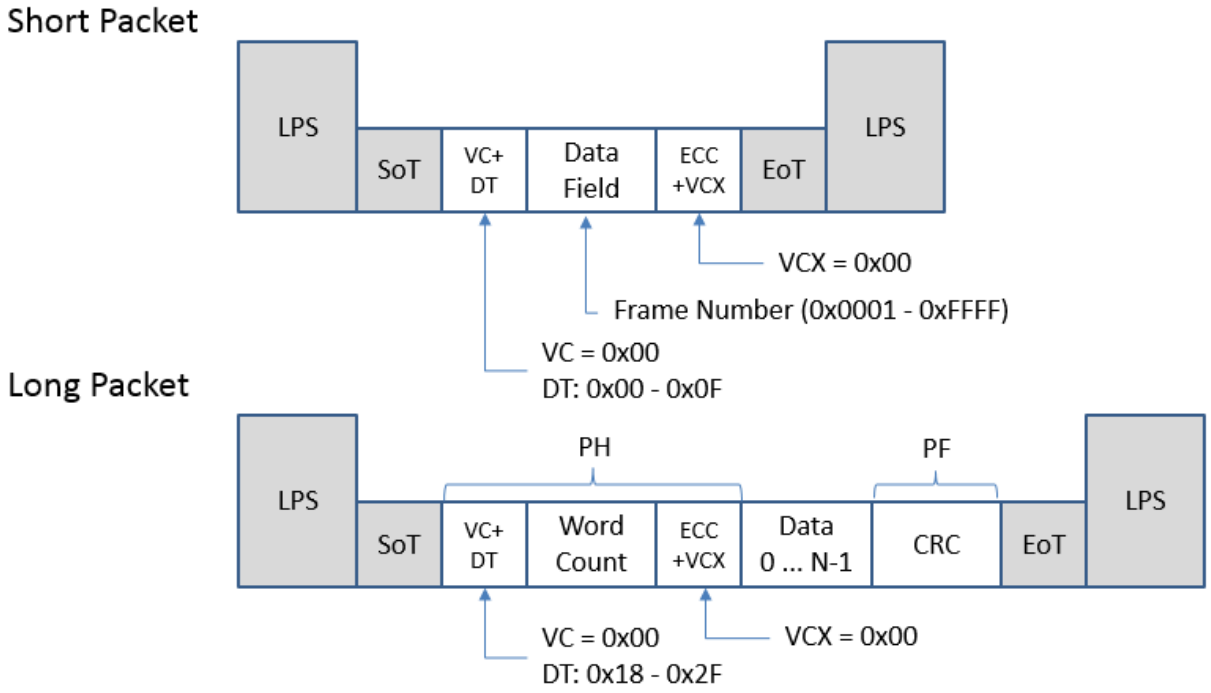
- The output image format is standard and corresponds to YUV and Raw format. It is possible to correspond to other formats, but it is necessary to consult.
- The USB 3.0 chip is equipped with Cypress EZ-USB FX3.
- It starts as a USB mode by setting the DIP SW number 8 to on and booting.

2.2. USB Mode Connection Configuration



2.3. Output format

The details of the MIPI CSI-2 signal output by this board are shown below. In addition, because it is possible to change the output format as a custom correspondence, please contact us.



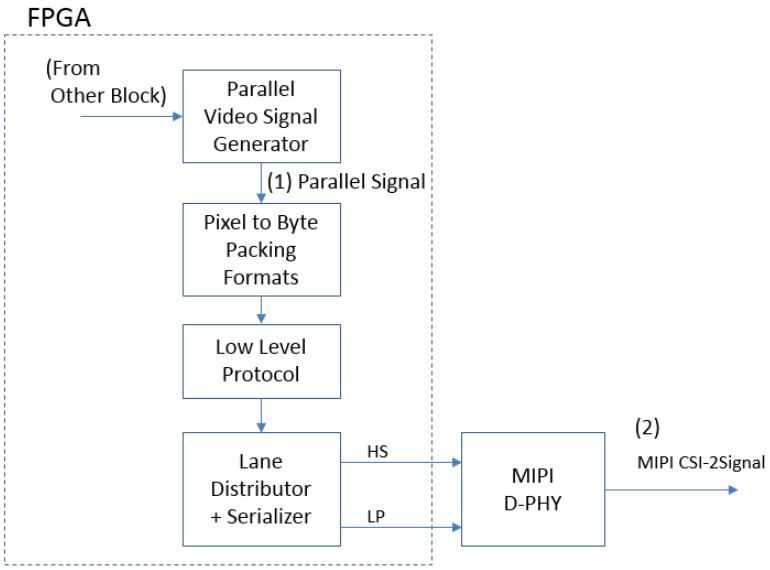
- Virtual Channel (VC) is 0x00-fixed.
- Line Start, line End Short Packet output is optional.

The following table shows the supported pixel formats and Data types for this board. The input AVI format column shows the pixel format of the input AVI file when this board is operated from SVOGenerator.

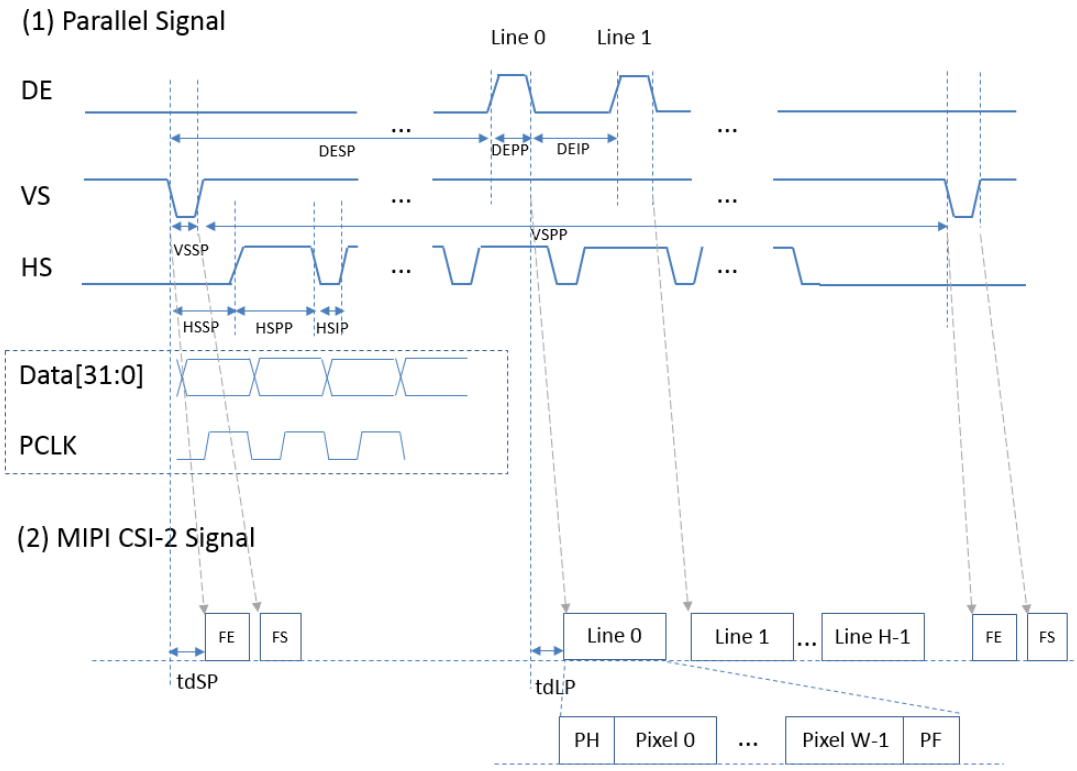
Pixel Format	Data Type (DT)	Input AVI Format (SVOGenerator)
YUV4:2:2 8-bit	0x1E	UYVY, YUY2
RGB24 (RGB888)	0x24	DIB (Upper and lower inverse)
Raw10	0x2B	UYVY
Raw12	0x2C	UYVY
Raw20	0x2F	DIB (Upper and lower inverse)

- Even if you have a DIB or RGB AVI data loaded, the first side of the AVI file will always be in the order of the data being sent.

2.3.1. SVO-MIPI Video Output Block

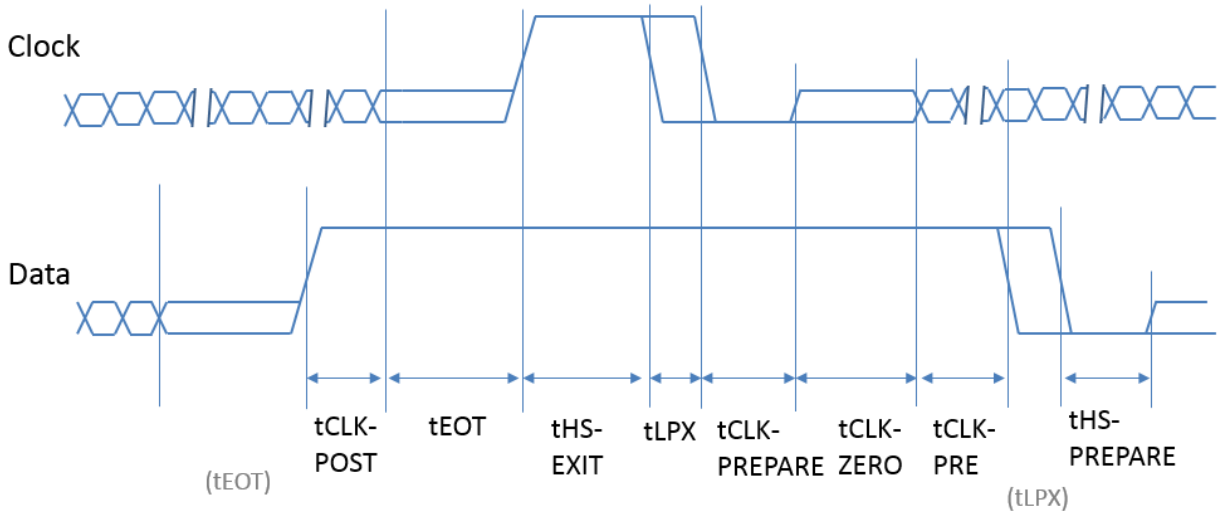


As shown above, the SVO-MIPI board has a two-stage video output block inside the FPGA. The first stage video signal generator generates a 32-bit parallel video signal, and the second stage MIPI signal converter Serializes the parallel video signal to the serial signal. The serial signal is outputted outside the board as a MIPI CSI-2 signal via the MIPI D-PHY. The timing relationship between the parallel signal and MIPI CSI-2 signal is shown below.



Timing	typ	max	Note
tdSP	75 ns		Defined by the value of the LP11-LP01 transition of the CLK Lane
tdLP	160 ns		Ditto; Measured at 1080p, 30fps, UYVY (inversely proportional to data rate)

2.3.2. MIPI Output Timing

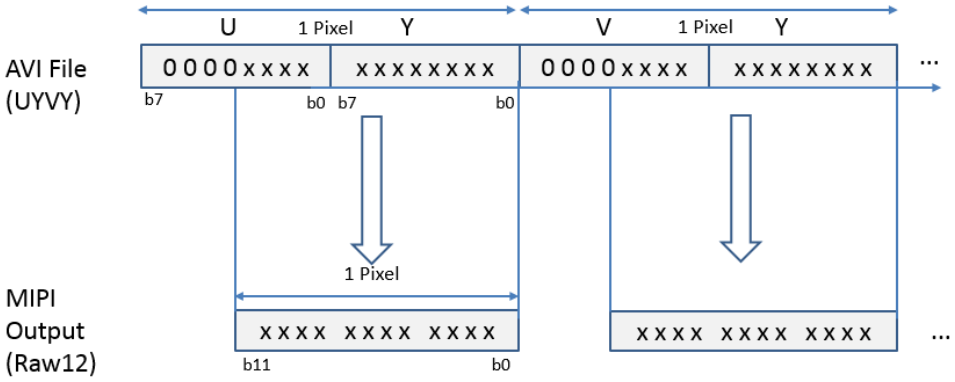


Timing	min	typ	max
tCLK-POST	60ns + 52UI	210 ns	
tEOT		60 ns	105ns + 12UI
tHS-EXIT	100 ns		
tLPX	50 ns	87 ns	
tCLK-PREPARE	38 ns	60 ns	95 ns
tCLK-PREPARE + tCLK-ZERO	300 ns	363 ns	
tCLK-PRE	8UI	118 ns	
tHS-PREPARE	40ns + 4UI	60 ns	85ns + 6UI

- The typical value indicates the measured value at the time of 800Mbps/lane output.

2.4. Processing on RAW output

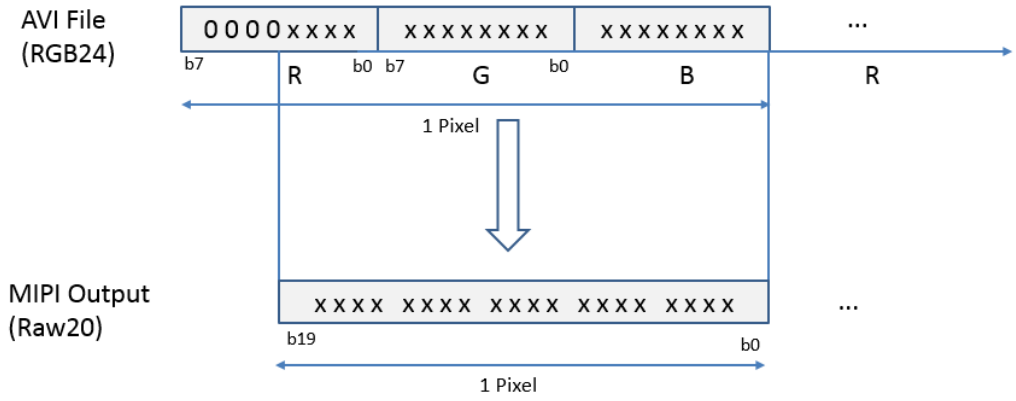
SVO-03-MIPI supports Raw output (RAW10/Raw12/RAW20). Because the Windows OS standard VFW does not support Raw video, if you select Raw output in USB mode, the input file will be in accordance with the format stored on our capture board such as SVM-MIPI. This means that some of the input data in the YUV or RGB format is considered to contain valid data and outputs the MIPI signal. The details of the data format are as follows.



On the host side, treat it as UYVY and ignore the upper bits.

(Bit rate is 4/3 times)

(If the above figure is raw12; RAW10 as well)



On the host side, treat it as RGB24, and the upper bits padding 0.

(Bit rate is 6/5 times)

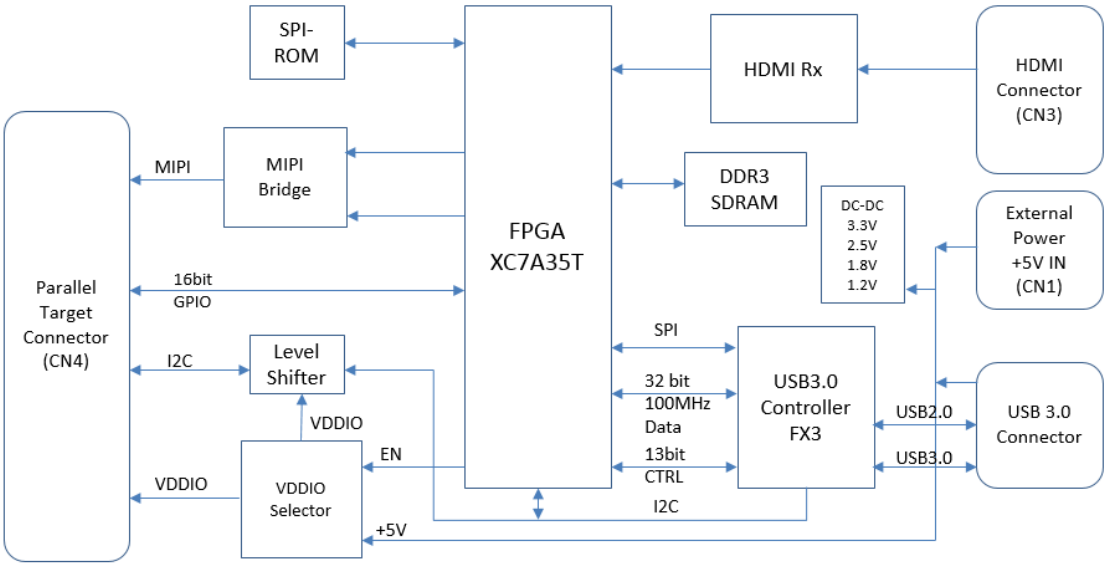
For RGB24 and RAW20 output, the input AVI file supports the RGB24 format. The order of the output pixels of the SVO-03-MIPI board is always identical to the byte array in the AVI file. In other words, if you emulate a standard camera using RGB24 AVI files, the VFW RGB24 (from bottom left to upper right) is different for the vertical direction of each frame in the AVI file. Data must be stored in the order from the top left to the bottom right. In other words, if you enter an AVI file in the RGB24 format that is reversed upside down, the output signal of the board will be output in the order of the upper left pixel and the lower right pixel.

3. SVO-03-MIPI Block Diagram

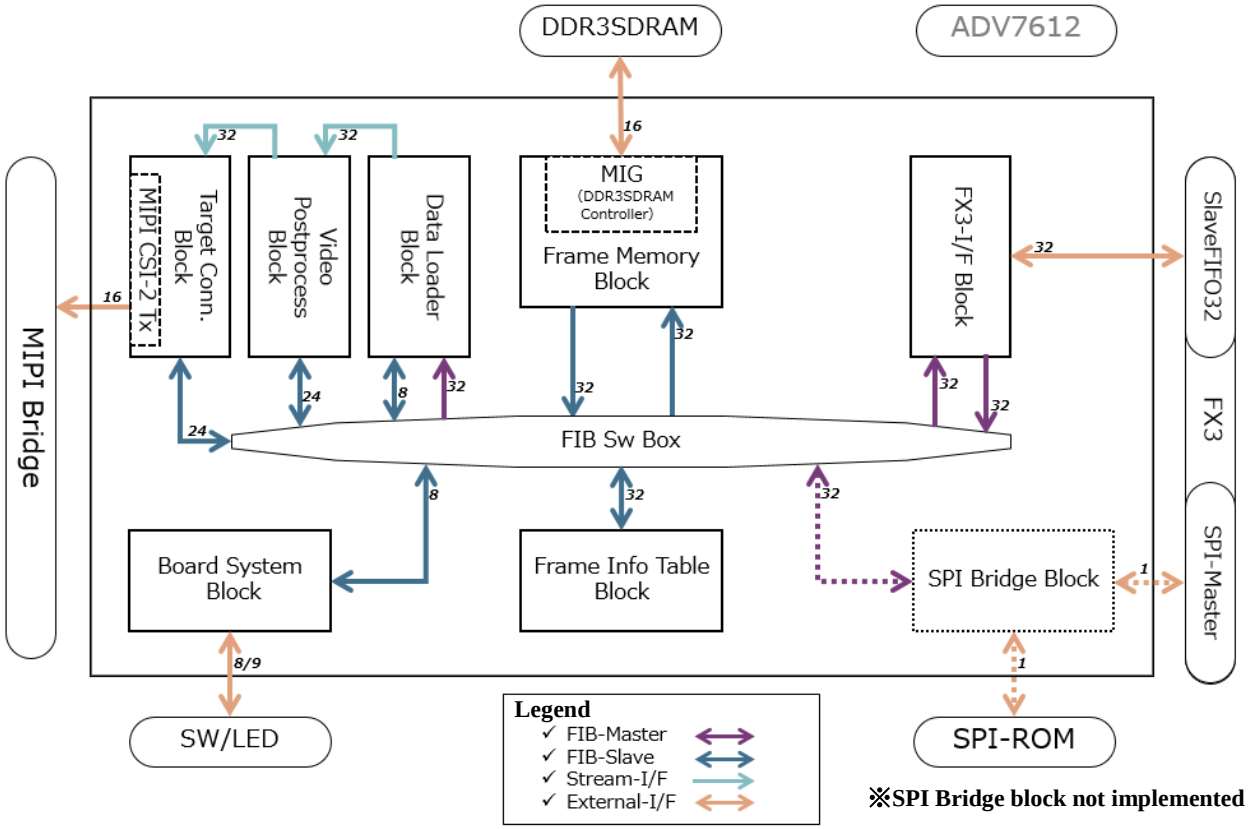
A schematic block diagram of the SVO-03-MIPI board is shown below.

3.1. Block Diagram

SVO-03-MIPI Block Diagram

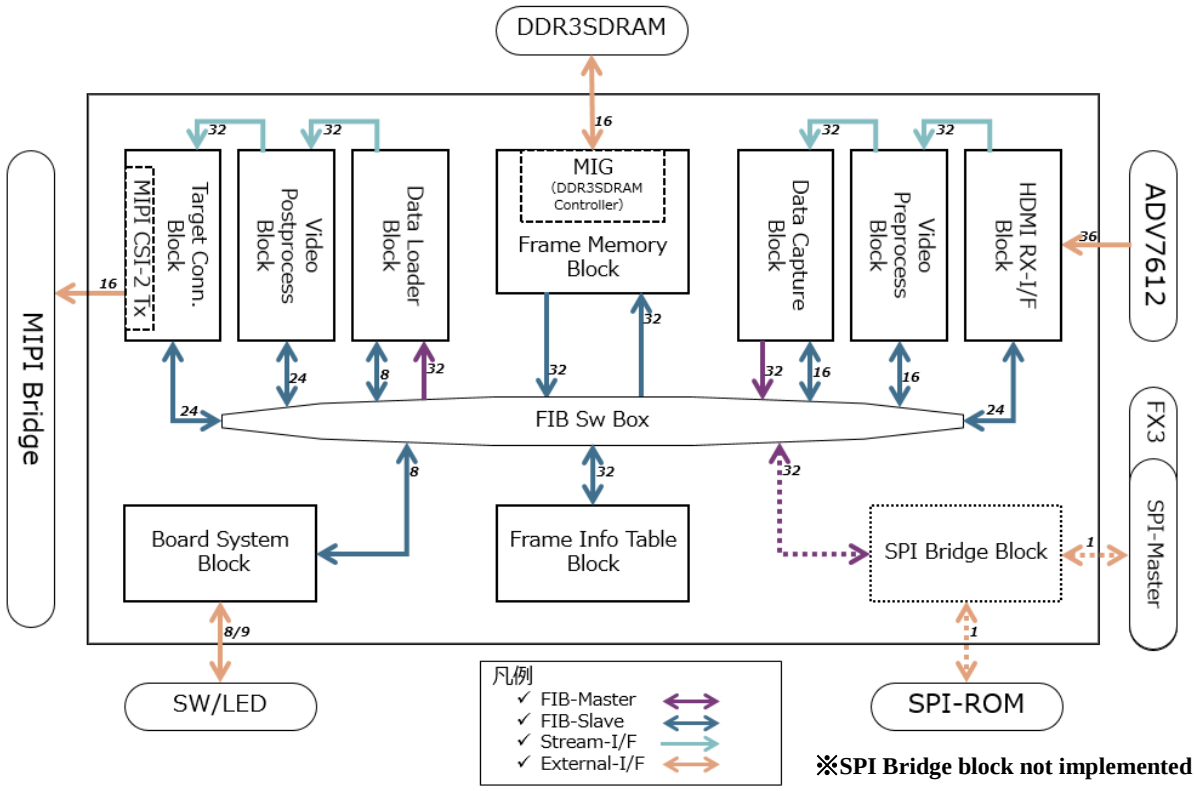


3.2. FPGA internal block diagram in USB mode



※SPI Bridge block not implemented

3.3. FPGA internal block diagram in HDMI mode

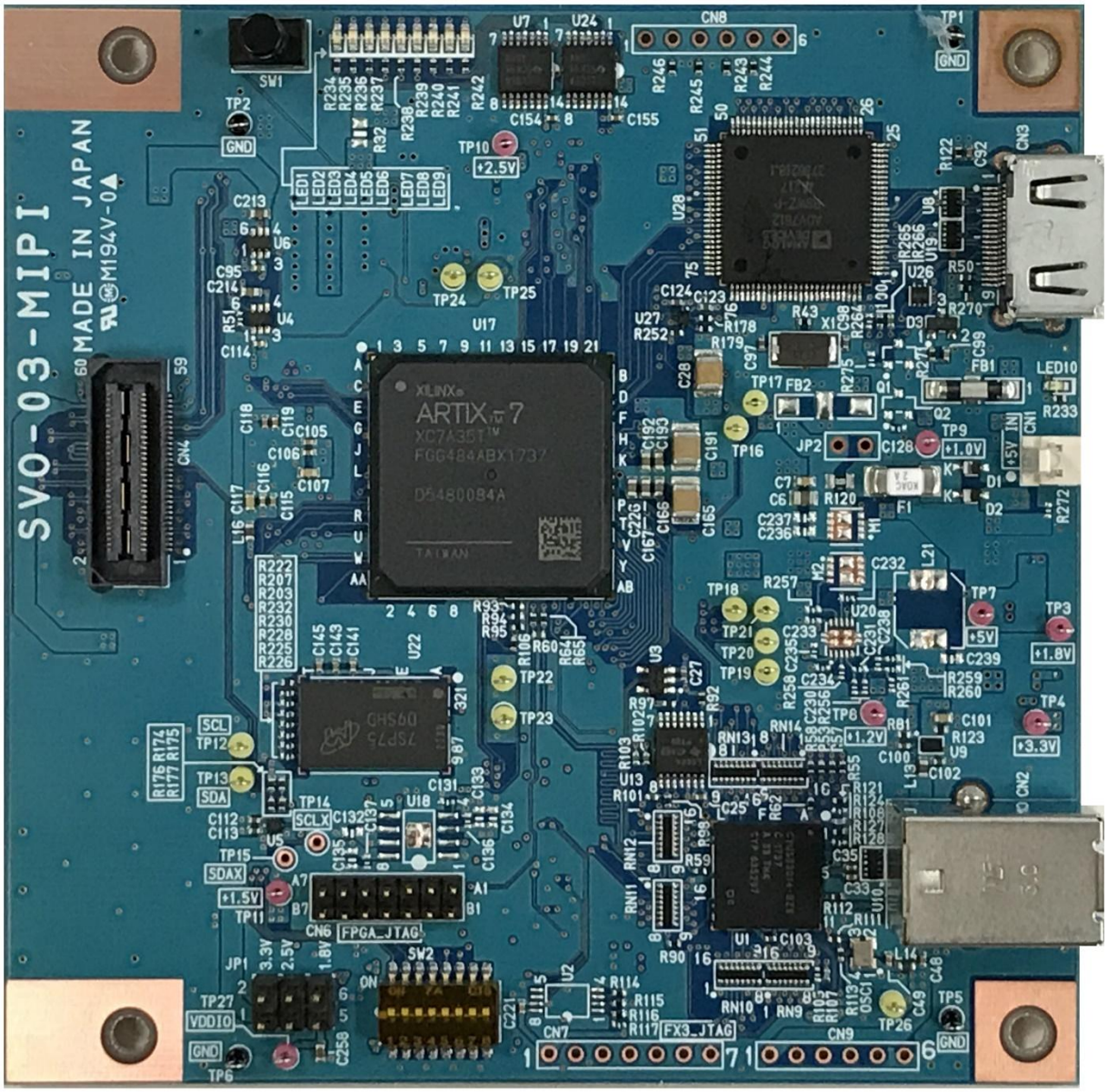


※SPI Bridge block not implemented

4. Exterior of SVM-MIPI Board

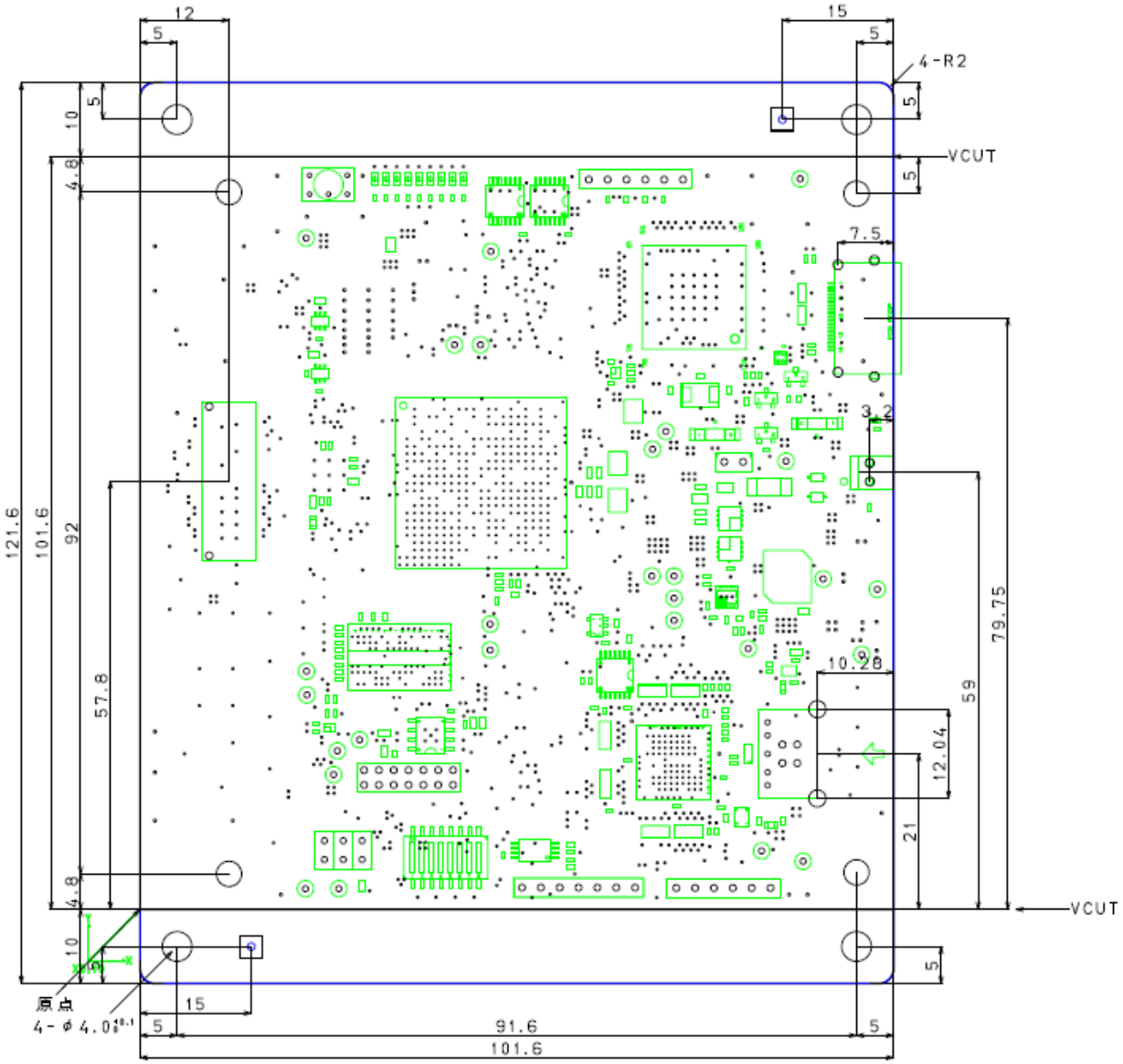
A photo and a picture of the outline of the SVO-03-MIPI board are shown below.

4.1. Photos



4.2. Drawing

The dimensions of the SVO-03-MIPI board are listed below. The actual board does not include 10mm parts up to VCUT at the top and bottom, and the vertical size is 101.6 [mm] in the same way as other SV series substrates.



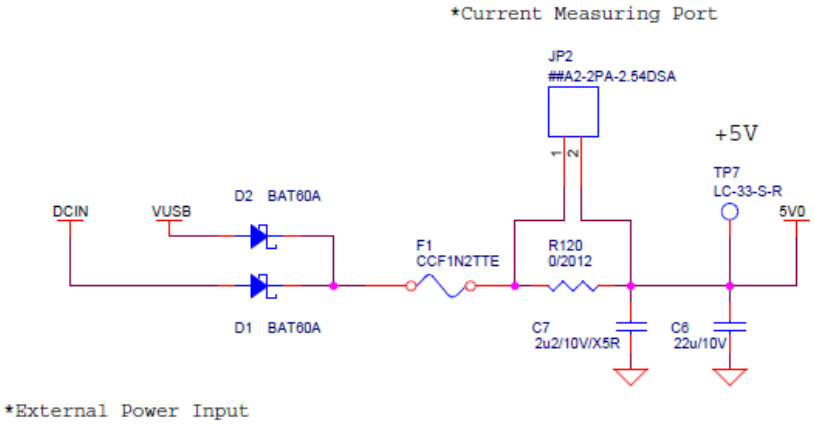
5. Connector Specification

This chapter describes the connector specifications that should be considered during normal use. In the Appendix section there are some specification about other connectors.

5.1. **CN1** : Sub Power connector

Power Connector for use when the USB bus power does not meet the power capacity or is not powered via USB bus power.

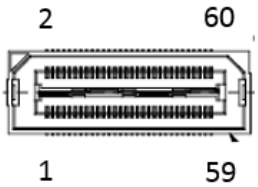
Connector		22-04-1021: Molex					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	+5V	IN	DC5V Input	2	GND	-	GND



- The + 5v (DCIN) from CN1, and the + 5v (VUSB) from the USB connector are connected by a diode or as shown in the circuit diagram, and are used as a board internal power supply (5V0).

5.2. **CN4** : Target Connector

This connector is used to connect the target image sensor.



Connector		QSH-030-01-L-D-A: SAMTEC					
Pin#	Name	DIR	Description	Pin#	Name	DIR	Description
1	D1_N	OUT	MIPI Lane 1 Output -	2	GPIO0	IO	GPIO 0 (Reserved) Trigger Signal/ FSYNC Signal Output 1
3	D1_P	OUT	MIPI Lane 1 Output +	4	GPIO1	IO	GPIO 1 (Reserved)
5	GND	-		6	GND	-	
7	D3_N	OUT	MIPI Lane 3 Output -	8	GPIO2	IO	GPIO 2 (Reserved)

9	D3_P	OUT	MIPI Lane 3 Output +	10	GPIO3	IO	GPIO 3 (Reserved) Trigger Signal/ FSYNC Signal Input 1
11	GND	-		12	GND	-	
13	CLK_N	OUT	MIPI Clock Output -	14	GPIO4	IO	
15	CLK_P	OUT	MIPI Clock Output +	16	GPIO5	IO	
17	GND	-		18	GND	-	
19	D2_N	OUT	MIPI Lane 2 Output -	20	GPIO6	IO	
21	D2_P	OUT	MIPI Lane 2 Output +	22	GPIO7	IO	
23	GND	-		24	GND	-	
25	D4_N	OUT	MIPI Lane 4 Output -	26	GPIO8	IO	
27	D4_P	OUT	MIPI Lane 4 Output +	28	GPIO9	IO	
29	GND	-		30	GND	-	
31	SCL	OUT	I2C SCL Signal Line	32	GPIO10	IO	
33	SDA	IO	I2C SDA Signal Line	34	GPIO11	IO	
35	GND	-		36	GND	-	
37	GND	-		38	GND	-	
39	GND	-		40	GND	-	
41	GND	-		42	GND	-	
43	VSYNC	OUT	VSYNC Output (Reserved)	44	GPIO12	IO	
45	HSYNC	OUT	HSYNC Output (Reserved)	46	GPIO13	IO	
47	GND	-		48	GND	-	
49	CK	OUT	Clock Output(Reserved)	50	GPIO14	IO	
51	RST	OUT	Reset Output (Reserved) （L : Reset）	52	GPIO15	IO	
53	GND	-		54	GND	-	
55	VDDIO	POW	IO Power Output	56	1V2	POW	1.2V Power Output
57	3V3	POW	3.3V Power Output	58	3V3	POW	3.3V Power Output
59	GND	-		60	GND	-	

- HSYNC, VSYNC, and GPIO pins are reserved for use during customization. There is no function in the standard version.（Hi-Z）
- 1.2 V and 3.3 V can be output to about 150mA.
- The IO voltages for each single-ended port are determined by the jumper JP1.
- SCL, SDA is connected via the level conversion IC to the I2C bus inside the SVO-03-MIPI.

6. Detail of each part

6.1. **SW1:** Push Switch

The current function is unassigned.

6.2. **SW2:** DIP Switch

This is a 8-bit switch for setting the various modes of operation of SVO-03-MIPI. The following settings can be set by the switch.

Number	Name	Turns OFF	Turns ON
1	（Reserved）	Normal Mode	
2	（Reserved）	Normal Mode	
3	（Reserved）	Normal Mode	
4	Board Number b0		
5	Board Number b1		
6	Board Number b2		
7	Update Mode Setting	Normal Mode	Update Mode (DIP SW #8: OFF)
8	Working Mode (effective when power up)	HDMI Mode	USB Mode

6.3. **LED1-9**: Working State Indicator

This LED displays the operating status of the board or FPGA.

LED#	Description
1	Indicates that the VDDIO power supply to the target are being supplied when lit.
2	Lights up when the LP state change of the CLK + Lane is detected.
3	Lights up when the LP state change of the D0 + Lane is detected.
4	Lights up when overflow is occurring in the MIPI output block.
5	Lights up when the pixel clock in the parallel signal generation block is locked.
6	Lights up when the clock in the MIPI signal generation block is locked.
7	When Internal integrated video Sync signal source is driving, the LED is switched ON/OFF at a cycle of 3-minute laps of the V-sync sync signal.
8	Light up when the Images that have been stored in frame memory is loaded for output to target. The lighting condition of this led does not necessarily indicate the image output to the target.
9	(USB Mode) Always goes off. (HDMI Mode) The LED is switched ON/OFF at a three-minute cycle of the V-sync signal from the HDMI receiver.

6.4. **JP1** ： VDDIO selection jumper

A jumper for selecting the IO Power (VDDIO) of the target device to be generated by the SVO-03-MIPI board. It can be selected from 1.8 V, 2.5 V, 3.3 V, and can output a current of about 150mA.

VDDIO is intended to be used as an IO supply voltage for image sensors and target devices. In addition, GPIO0-15, CLK, RST, and SCL, and SDA signal lines are input and output of the VDDIO power level.

In default, VDDIO is set to 3.3V.

7. Check Terminal

7.1. **TP27:** VDDIO check terminal (red)

This is the check terminal used to adjust the VDDIO.

7.2. **TP3-4, 7-11:** Voltage check terminal (red)

This is check terminal for each supply voltage required by the SVO-03-MIPI board operation. In normal use, there is no need to check. Also, please stop extract the power from this check terminal to supply power to external modules.

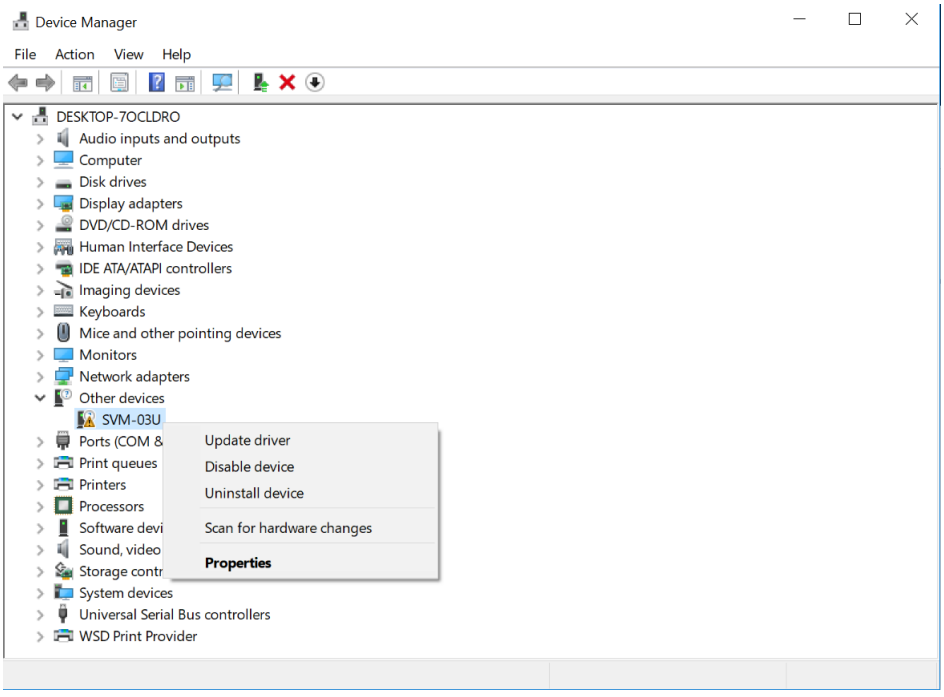
7.3. **TP1,2,5,6:** GND check terminal (black)

Please use it as a GND terminal.

8. Update the Board

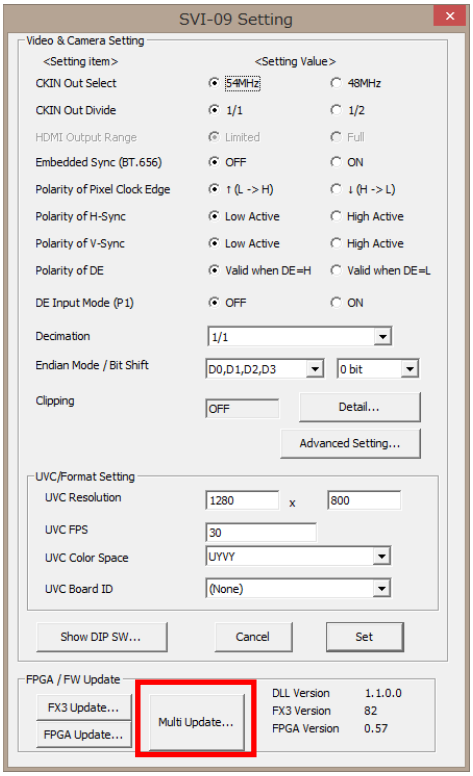
The SVO-03-MIPI board can update firmware and FPGA configurations via USB. The update procedure is as follows.

1. Connect the SVO-03-MIPI board to the PC, with DIP SW (SW1) number 7 ON and number 8 OFF.
2. Because it works with a different driver than the USB mode, you should install the driver manually from Device Manager when you first start it.
    1. "Other devices" → "SVM-03U" and click "Update driver"



    2. Click "Browse your computer to find driver software"
    3. Select the driver folder (Driver_SVI or Driver_SVM) and click “Next”.
3. Start "SVMCtl" and click "SVM Setting...".

4. Select "Multi Update..." and select the update image to start the update.



5. The update will take several minutes. Do not unplug the USB cable or turn off the PC.
6. When the update message exits, exit "SVMCtl" and unplug the USB cable.
7. The DIP SW is restored and the update is complete.

9. Applicable version

Mode	FX3 Version	FPGA Version
USB Mode	N/A	0.20
HDMI Mode	N/A	N/A

10. Notes

For proper use of this board, be sure to follow the following precautions.

1. The firmware/FPGA update is done using the SVM-03 control software (SVMCtl) from the host PC.
2. When you connect or take off the target, make the power supply of the SVO-03-MIPI board state of “OFF" by all means.
3. It isn’t guaranteed that all HDMI monitor can display by each output image size and frame rate setting. Capable of outputting setting is differs from among monitors, nothing may be displayed in the output form that is not supported.
4. About power supply for this board, please use the power supply which has enough current capacity. Please supply power supply from PC under the self-responsibility of the customer. If you broke PC by any chance, we can’t take any responsibility..
5. The contents of this document may be changed in the future without notice.
6. Reprinting of part or the whole of the contents of this document is strictly forbidden.
7. Through extreme care has been taken in preparing this document, if you find any ambiguous points or errors, or if you would like to make any comments on the document itself or its content, please contact to sv-support@net-vision.co.jp.
8. Be sure to use the newer SVMCtl utility software than the version that came with the CD-ROM. If you rewrite the SPI-ROM using a previous version of this board, it may not work due to false detection of the board.