High-Grade MIPI Input Video Capture Board

[SVM-06]

Hardware Specification

Rev.1.0

NetVision Co., Ltd.

Update History

Revision	Date	Note	
1.0	2020/04/09	New File（Equivalent to Japanese version 1.4）	H. Suzuki

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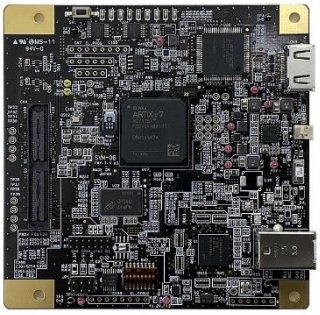
1. Overview



This document is a hardware specification of the board **"SVM-06"** to convert the MIPI CSI-2 standard video signal from an image sensor to an HDMI or USB 3.0. The SVM-06 is a board developed as a high-performance version of our existing MIPI capture board SVM-MIPI.

SVM-06 operates according to the operation mode specified by DIP SW (SW2) on the board. In the standard specification of SVM-06, there are three modes, **"HDMI mode", "UVC mode" and "Updater mode"**. In addition, it is also possible to add a vendor output mode equivalent to our SVI-09 and a MIPI output mode equivalent to our SVO-03-MIPI as custom support.

In HDMI mode, you can connect to a target such as an image sensor, connect it to a PC monitor or TV with an HDMI port, and easily display and verify and evaluate the image data from the target in real time on the monitor. Equipped with a 300MHz TMDS HDMI transmitter, it can output video images up to 4K 30fps or 1080p 120fps. Moreover, since the USB port operates in the following UVC mode at the same time, it is possible to simultaneously capture video from a PC via USB3.0 while checking the video with HDMI.

In UVC mode, you can capture from your PC as a device that complies with UVC (USB Video Class), so you can evaluate image sensors and develop algorithms on various OSs such as Windows and Linux. Uncompressed video data can be transmitted at a maximum bandwidth of 3 Gbps, since the data is transferred to the PC via USB3. It can be easily connected to third-party software such as OpenCV and ROS because it is a UVC-compliant device that does not require a device driver. The same operation as this mode is possible in the HDMI mode, but this mode consumes less power. So please use this mode when using only the USB port.

In the updater mode, you can update the firmware of devices such as microcomputers and FPGA on the board via USB. The board cannot be updated in HDMI mode or UVC mode, so be sure to start in update mode when update it.

1.1. SVM-06 Functions

HDMI mode: MIPI Video Signal -> HDMI Conversion (Simultaneous output to USB3.0)

UVC mode: MIPI Video Signal -> USB3.0 (UVC) Conversion

Updater mode: Update the firmware of the board

1.2. Specifications (HDMI Mode)

Power: USB Bus Supply (External Power Input Applicable) / +5V 0.9A typ.

Input Standards : MIPI CSI-2 Video Signal (1 - 4 lane)

Data rate per lane: max. 1.5 Gbps

Effective pixel data rate: max. 6.0 Gbps

Input Resolution: max. 8190 x 4095 pixel

Input Pixel Format: YUV4:2:2, Raw8, Raw10, Raw12

Output (1): HDMI Connector (YUV4:2:2 8bit or RGB24)

Output (1) Resolution: 1280x720 / 1920x1080 / For custom, max. 8190x4095

- Can be cut out in any area

Output (1) Frame Rate: 30 FPS / 60 FPS / For custom resolution, supports any frame rate

Output (1) Data Rate: max. 7.2 Gbps (Equipped with 300MHz TMDS transmitter)

Output (2): USB 3.0 (Details follow UVC mode)

- In the case of Raw input, the image is output as a monochrome image (Pixel-by-Pixel) in HDMI mode.

- If you want raw input and color output, please contact us.

- Contact us for how to set the custom resolution function.

1.3. Specifications (UVC Mode)

Power: USB Bus Supply (External Power Input Applicable) / +5V 0.5A typ.

Input Standards: MIPI CSI-2 Video Signal（1 - 4 lane）

Data rate per lane: max. 1.5 Gbps

Effective pixel data rate: max. 6.0 Gbps

Input Resolution: max. 8190 x 4095 pixel

Input Pixel Format: YUV4:2:2, Raw8, Raw10, Raw12

Output: USB 3.0 (USB 2.0 is possible if it is about VGA size)

USB Device Class: USB Video Class (UVC)

Output Through Rate: max. 3.0 Gbps

Output Resolution: Same as input resolution

- Can be cut out in any area

Output Frame Rate: Any

Output Pixel Format: YUV4:2:2, RGB24

- In the case of Raw input, all data is output by assigning it to the pixel format YUV 4: 2: 2, and the dedicated capture software enables monochrome and color display.

1.4. Board Specification Table

Items	Contents	Remarks
Video Input Interface	MIPI CSI-2 video signal FPD-Link III / GMSL / GVIF2 (In case of connection with our deserializer boards)	Supports Non-Continuous / Continuous Clock Max. 8 data lanes + 2 clock lanes. In the standard specification, only 4 lanes + 1 clock lane can be used.

			For custom, 2 system inputs or 1 input + 1 output are available.
Video Output Interface		UVC (USB Video Class) / HDMI 1.4	Supports Windows / Linux
Input Resolution		Max. 8190 x 4095 pixel Within 6.0 Gbps	
Output Resolution		Max. 8190 x 4095 pixel (UVC mode) Within 3.0 Gbps (HDMI mode) Within 7.2 Gbps	(Standard resolution in HDMI mode) 1280 x 720 / 1920 x 1080 / 2560 x 1440 / 3840 x 2160 In UVC mode, make sure that the effective data rate in the frame is within 3.0 Gbps.
Sync Signal		FS / FE	
MIPI Data Lane		1, 2, 3, 4 lanes	
Data Rate per Lane		1.5 Gbps	
Supported Pixel Formats		YUV4:2:2 8bit / RGB24 / Raw8 / Raw10 / Raw12	
Other IF	I2C	1 system	SCL frequency 100 / 200 / 400 kHz
	GPIO	16 bit	IN / OUT can be switched for each bit
Input Power		+5V (±5%)	Use either USB Bus powered / 2-pins connector
Output Power		VDDIO output (1.8V, 2.5V, 3.3V) 5V, 3.3V, 1.2V output	
Other Functions		Test pattern output function Image clipping function (When ROM startup) Automatic transmission of I2C at startup	We can individually support Virtual Channel, Embedded Line.
Interface Connector		120pin (QSH-060-01-L-D-A)	Connectable with 60pin for our SVM-MIPI
FPGA		Artix-7 (XC7A35T) CrossLink (LIF-MD6000)	
Frame Memory		256MB (DDR3 SDRAM)	
USB3.0 Chip		Cypress EZ-USB FX3	
HDMI Chip		SiI1136	
Board Dimensions		101.6 x 101.6 x 25.7 [mm]	length x width x height
Attached Software (Windows)		NVCap (Capture Software) SVMCtl (I2C control / utility software)	

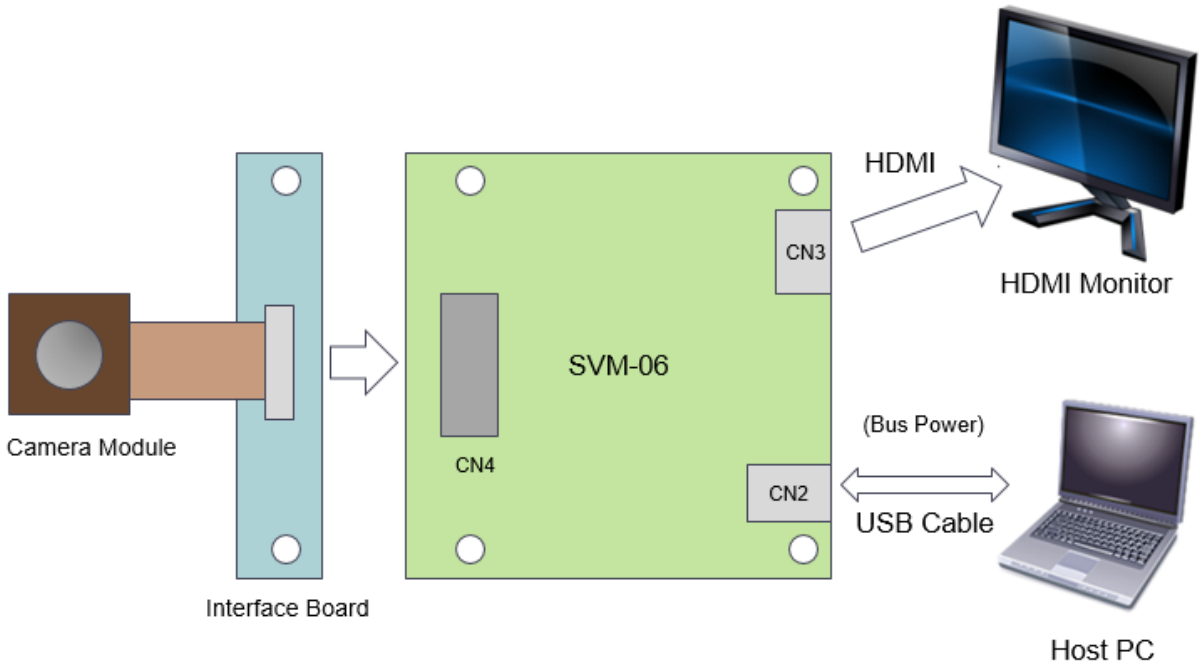
Supported Ser / Des board Examples	FPI-954-F GMI-9286-F GMI-9288-F GVI-4960-F and so on	

2. HDMI Mode Operation Details

This chapter describes HDMI mode (MIPI input, HDMI output).

When the power is turned on with the DIP SW on the board set to 8: OFF and 7: OFF, it starts in HDMI mode.

2.1. Connection Example in HDMI Mode



2.2. Input Format Settings

There are three input settings that need to be explicitly set in HDMI mode: the number of MIPI lanes, resolution setting, and clipping setting.

Since the number of MIPI lanes is set by the DIP SW on the board, refer to the DIP SW setting described later. The resolution setting and clipping setting are set via USB with the PC software (SVMCtl). The settings are saved in the SPI-ROM on the board, and they are reflected by reading the contents of the SPI-ROM at startup.

The resolution setting is the resolution specified in "UVC Resolution" of "SVMCtl", so specify the resolution of the input image or after clipping. Clipping setting is necessary, when you want to enable the clipping function that outputs only a part of the input image. Set the resolution of the clipping setting to be equal to the HDMI output resolution.

Refer to the software manual for details on how to make settings on your PC.

2.3. Output Format Settings

The HDMI output format is set by DIP SW on the board or software (SVMCtl). The output format can be selected from a standard format built into the firmware or a custom resolution that can be freely set by the user.

When outputting in the standard format (1080p or 720p), it can be operated only by setting the DIP SW on the board. Select 1080p / 720p and YUV / RGB output from the DIP SW according to the resolution of the monitor or image sensor you use.

For custom resolution, by written resolution timing data from your PC to the board using SVMCtl tool, and then it output to HDMI at any resolution up to about 8000x4000. The format supports YUV4: 2: 2 8bit or RGB 24bit. You use the data created by our SVO board tool "SVOGenerator" as the timing data.

When the custom resolution timing data has been written, the DIP SW resolution setting is ignored. To enable the DIP SW resolution setting, it is necessary to delete the custom resolution data with SVMCtl.

Besides, detailed settings such as input / output range settings can be set with SVMCtl. Refer to the SVMCtl software manual for details.

2.4. Notification about Power Supply

SVM-06 consumes about 800mA on 5V line, when it outputs test pattern without target connection. When target is connected, the power consumption may be larger. Please use sufficient AC adapter or USB cable. In UVC Mode, the power consumption is about 500mA.

2.5. Notification about USB Bus Power Supply

SVM-06 can work by USB power supply from a PC, but the USB specification has its limitations : The maximum is 500mA for USB2.0 port and 900mA for USB3.0 port. Thus, we don't offer a guarantee of operation when you use from USB bus power. Please use it at your own risk.

2.6. When Input Resolution and Output Resolution are Different

When the input resolution is larger than the monitor resolution, a part of the input video is cut out and output. In this case, it is necessary to specify the cutout area with your PC (SVMCtl tool). On the other hand, when the input resolution is smaller than the monitor, the input video is displayed in the center of the output screen and surrounded by black background. The function to enlarge and reduce the image is not implemented.

Please note that this operation is different from one in HDMI mode for such as SVM-MIPI (when the cutout area has not specified, the input resolution is automatically recognized and displayed in the center of the screen).

2.7. Processing on RAW Input

For Raw input formats, SVM-06 supports input of Raw8 / Raw10 / Raw12 format, but in HDMI mode it is output as a monochrome image of 1 pixel (dot-by-dot) per input pixel. Only the upper 8 bits are output and the lower bits are truncated. Raw image development (de-mosaic, color display) functions are not implemented.

2.8. Simultaneous Output to USB

In HDMI mode, it is possible to output data to HDMI and USB simultaneously. Basically, video format settings such as clipping settings are common to HDMI mode, and the USB side operates in the same way as UVC mode. However, it is possible to make different settings for UVC mode and for HDMI mode by directly setting the FPGA register. Contact us for details.

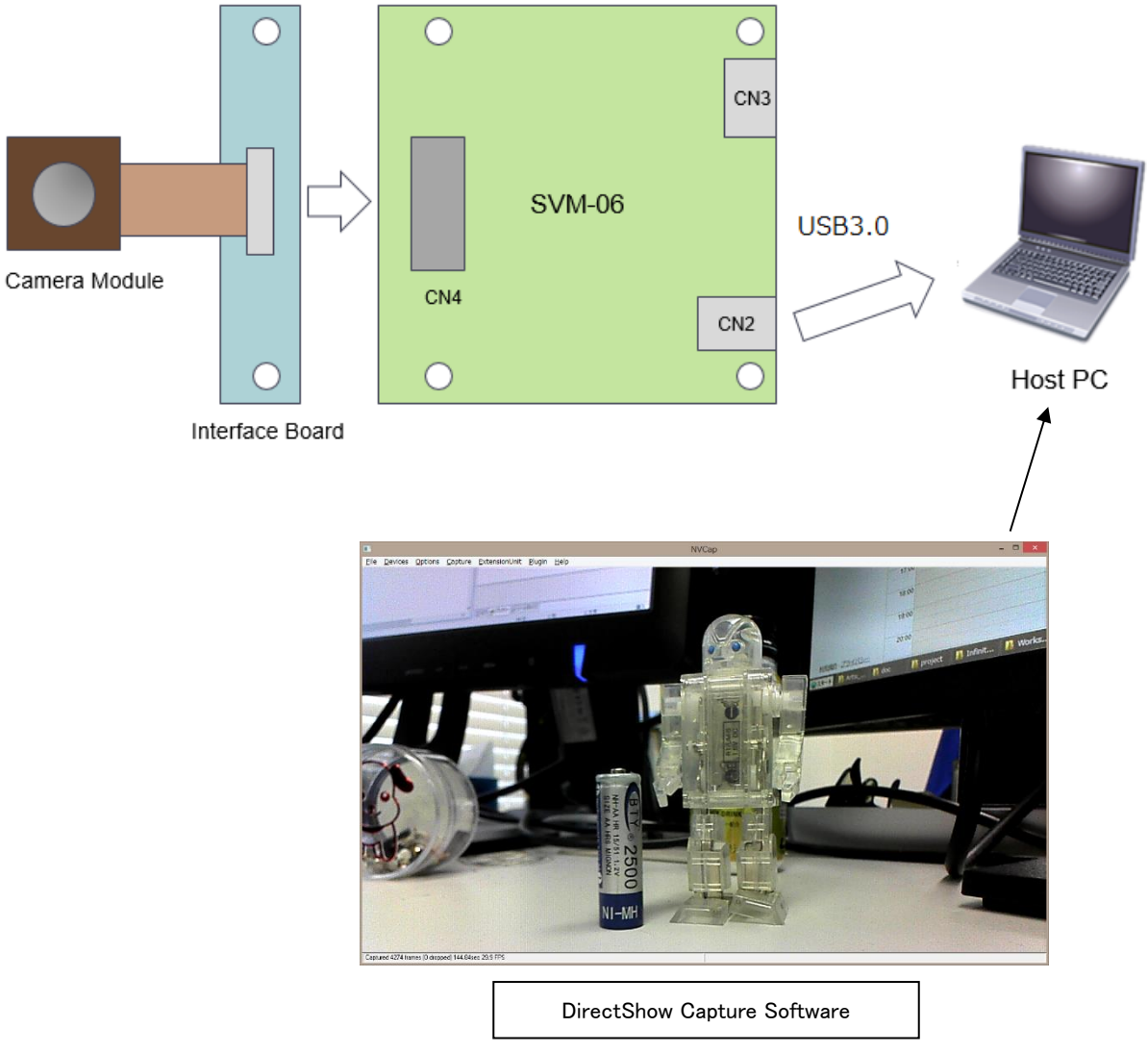
At present, the USB simultaneous output function cannot be used if the video input data rate is faster than the USB specification.

3. UVC Mode Operation Details

This chapter describes UVC mode (MIPI input, USB output).

When the power is turned on with the DIP SW on the board set to 8: ON and 7: OFF, it starts in UVC mode.

3.1. Connection Example in UVC Mode



DirectShow Capture Software

3.2. Format Settings

In UVC mode, the resolution, frame rate, and output pixel format settings are required in addition to the number of MIPI lanes and clipping settings common to HDMI mode.Since the number of MIPI lanes is set by the DIP SW on the board, refer to the DIP SW setting described later. Clipping setting is necessary, when you want to enable the clipping function that outputs only a part of the input image. This is set with the PC software (SVMCtl), and saved in the SPI-ROM on the board, Refer to the software manual for details.

Settings for only the UVC mode, such as resolution and frame rate, are set with SVMCtl. Set the resolution and frame rate according to the input video. If you use clipping function, you should set the resolution to the clipped one. The output pixel format is set according to the input pixel format of the MIPI signal. UVC supports three types of uncompressed video resolutions as standard: UYVY, YUY2, and RGB24. Therefore, when raw signal is input, all bits of raw signal can be captured by selecting UYVY or RGB24. Contact us if you need to support other output pixel formats.

3.3. Initial Setting Procedure in UVC Mode

As described above, in UVC mode, the initial settings are required at the time you first use according to the specifications of the image sensor. If this setup differs from the specification of the image sensor, it could not be captured normally.

1. Setting Target Power Voltage (VDDIO)

Before connecting the target device, VDDIO must be adjusted to the IO voltage of the target device. VDDIO can be switched by the jumper pin (JP1) on the board. The default setting is 3.3V.

2. Setting DIP SW

DIP SW should be set according to the number of MIPI lanes of the target device. The default setting is four lanes. Refer to section 7.2 for the detailed setting of DIP SW.

3. Initial Setting with PC

You need to set initial settings such as resolution and pixel format on your PC. You configure these settings with the software "SVMCtl" included on the CD-ROM. For details on how to operate SVMCtl, refer to the "SVMCtl Software Manual" on the CD.

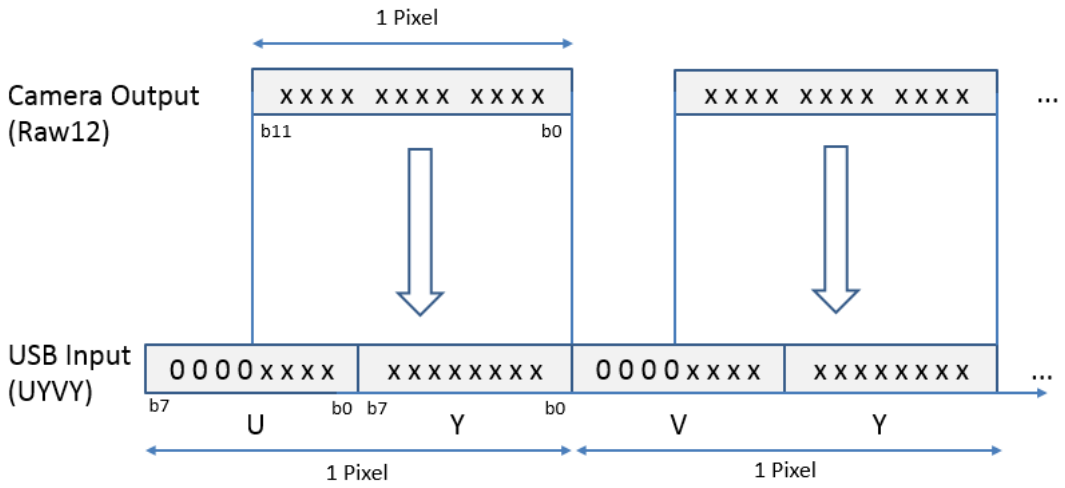
The factory settings follow ones described in the shipment report. The standard settings are as follows:

Resolution: 1920x1080
Frame Rate: 30 FPS
Color Space: UYVY

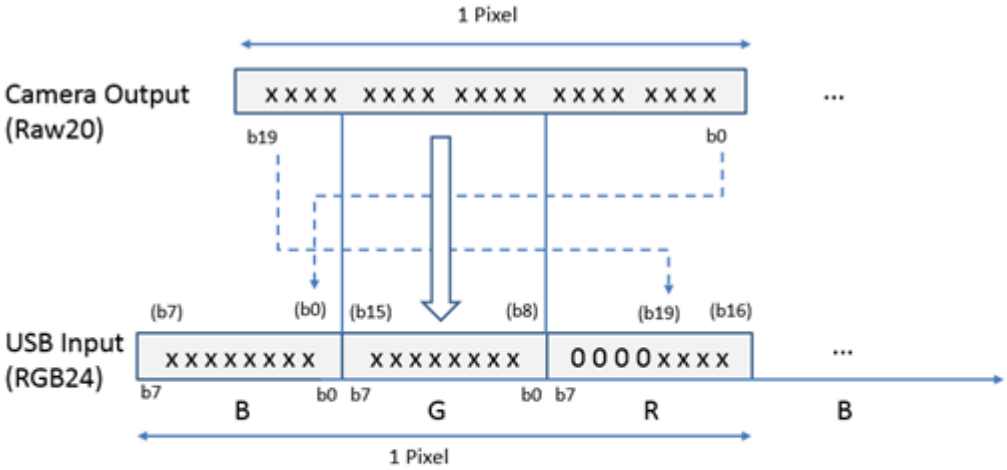
- SVMCtl may be updated from time to time. You can download the latest version from our website.
- The PC recognizes it as a device named "SVM-06".
- If the device name is assigned with SVMCtl, the ID number is added in parentheses after the device name.

3.4. Processing on RAW Input

For Raw input formats, SVM-06 supports input of Raw10 / Raw12 / Raw20 format. However, the UVC standard does not support Raw format. So, in UVC mode, in the case of Raw10-Raw12, the input data is regarded as 16 bits wide, and then the upper bit is set to 0 and output to the PC. Therefore, if you want to capture video of Raw10-Raw12 format, you should pack it into 16bit/pixel by specifying UYVY in the pixel format setting and import it. After that you can do the Raw image processing with the software on the PC.



In the case of Raw20, the input data is regarded as 24 bits wide, and then the upper bits are set to 0 and output to the PC. If you want to capture video of Raw20 format, you should pack it into 24bit/pixel by specifying RGB24 in the pixel format setting and import it. After that you can do the Raw image processing with the software on the PC.



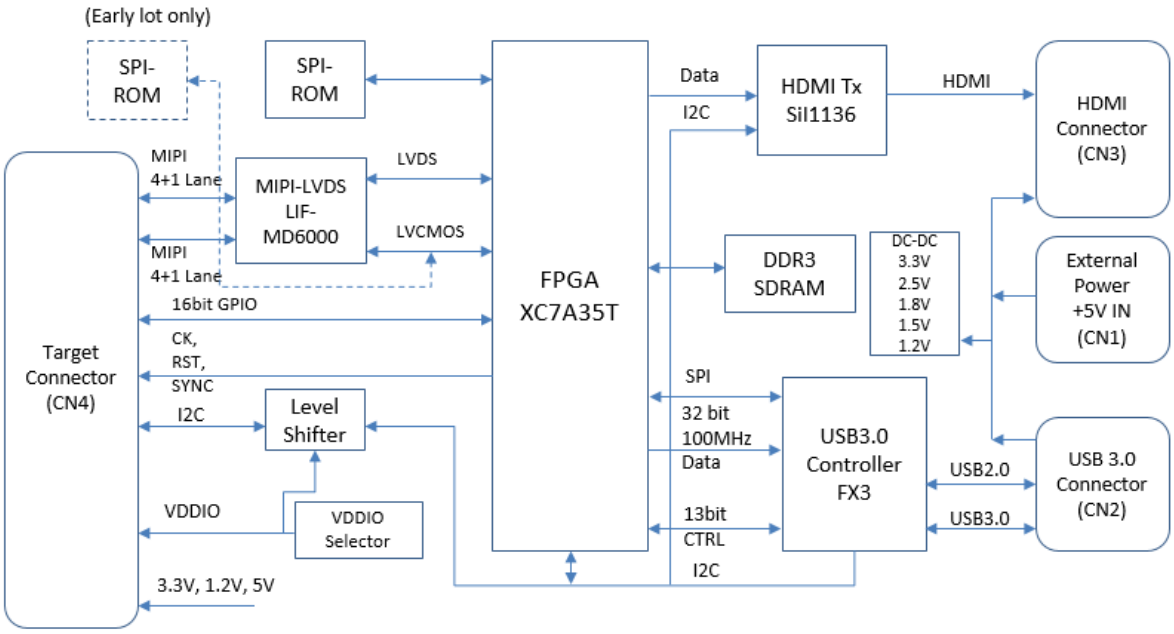
The host side treats it as RGB24 and the upper bits are set to 0.

(Bit rate is 6/5 times)

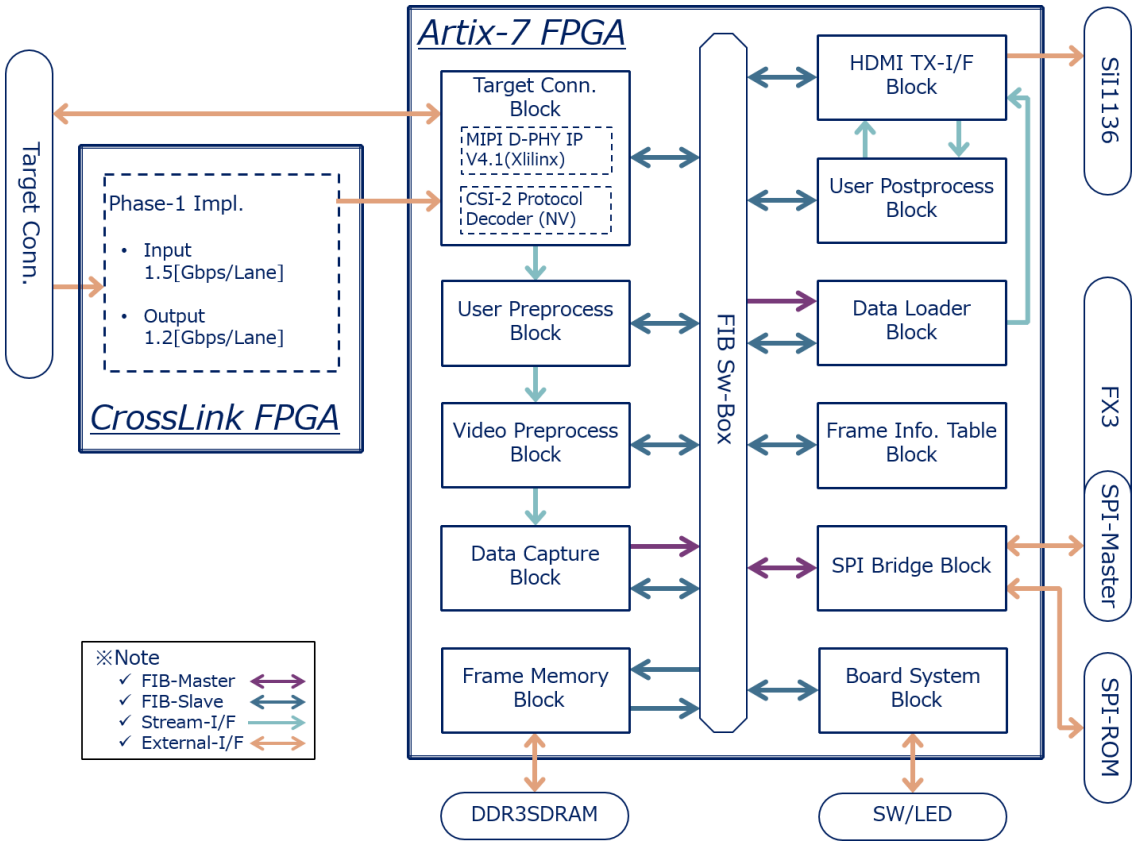
4. Block Diagram of SVM-06

A schematic block diagram of the SVM-06 board is shown below.

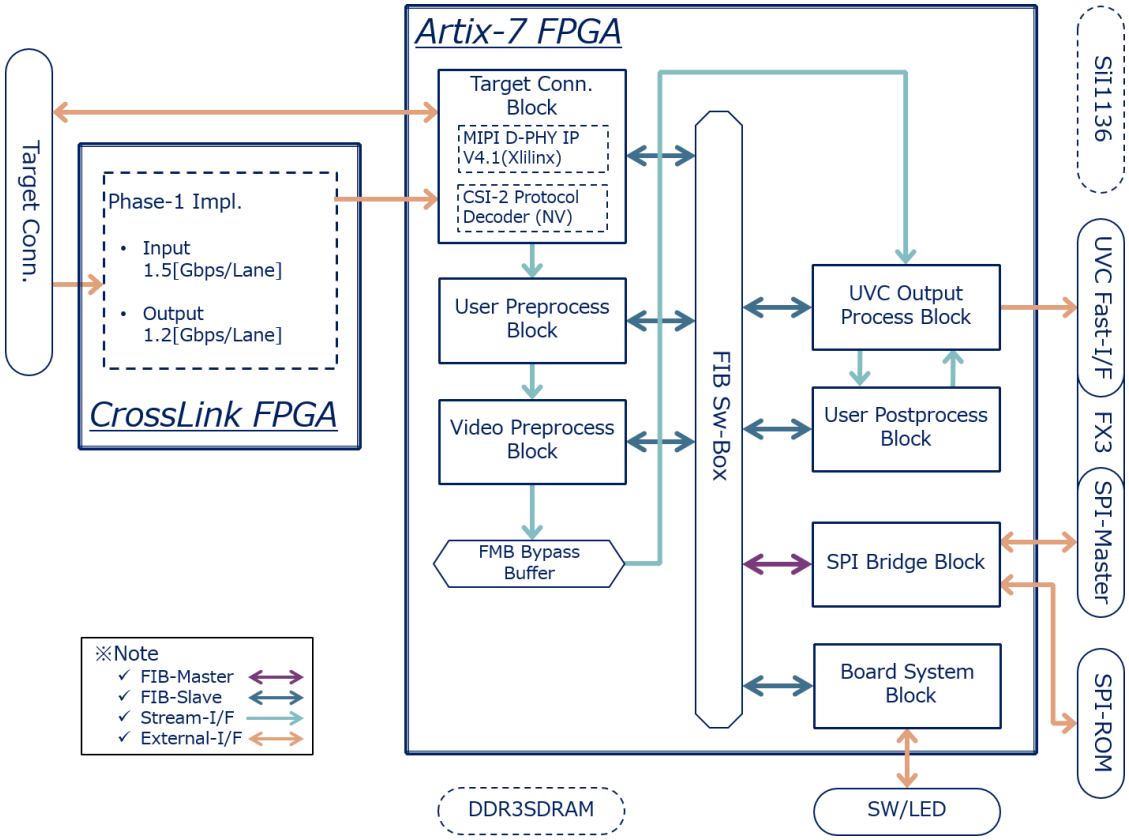
4.1. Block Diagram



4.2. FPGA Internal Block Diagram in HDMI Mode



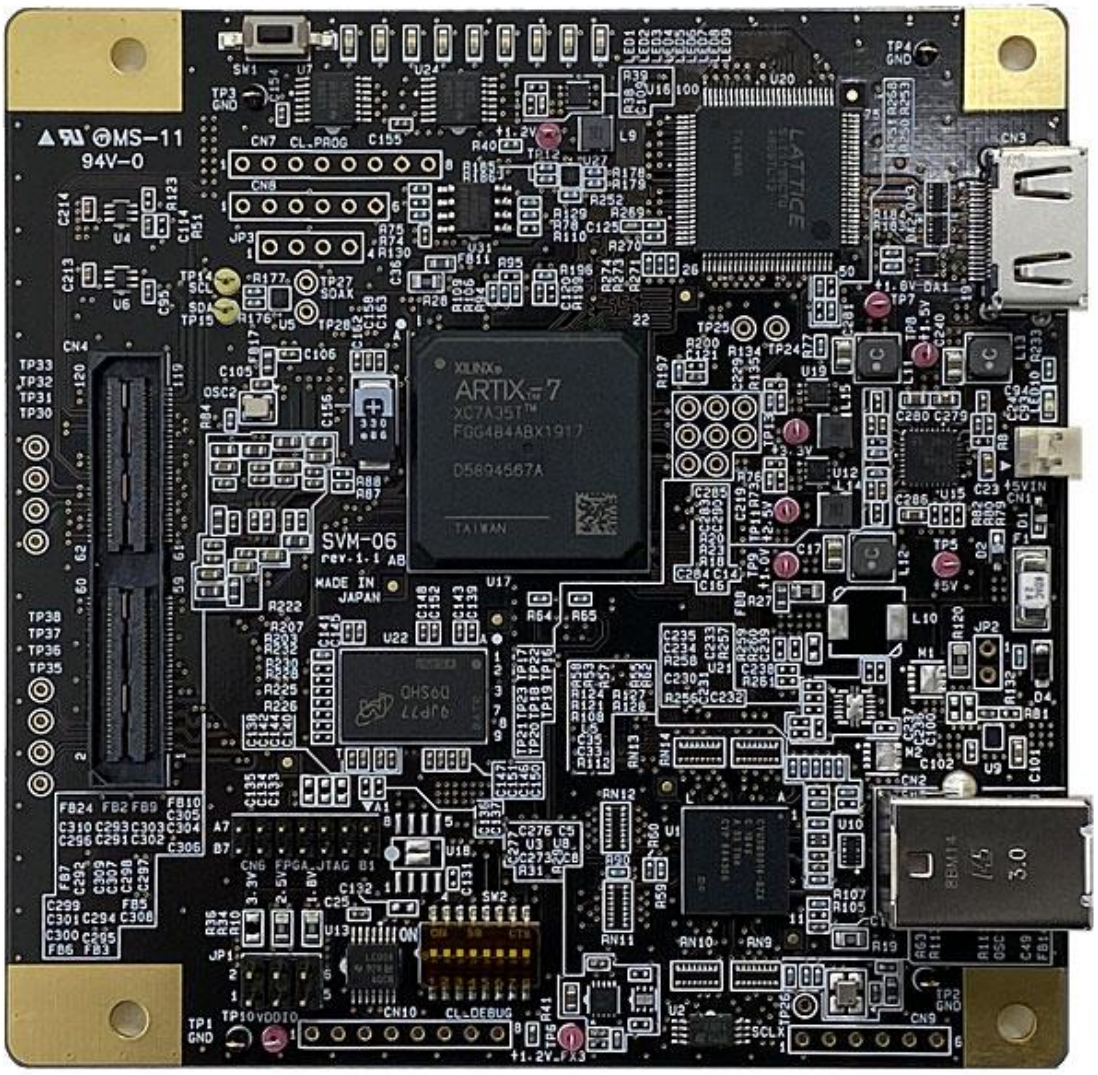
4.3. FPGA Internal Block Diagram in UVC Mode



5. The Shape of The Board

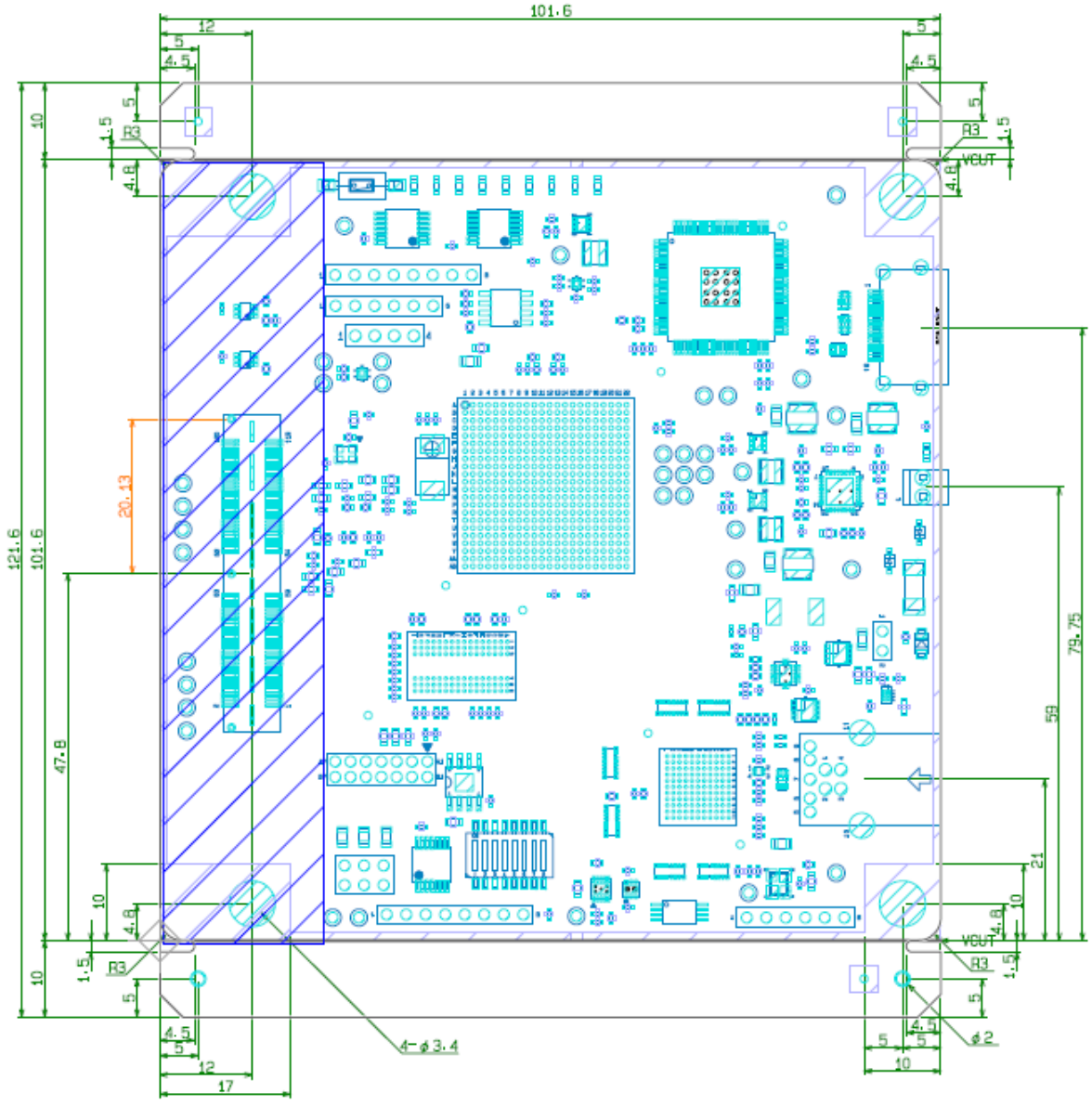
The photo and the picture of the outline of the SVM-06 board are shown below.

5.1. The Photo of The Board

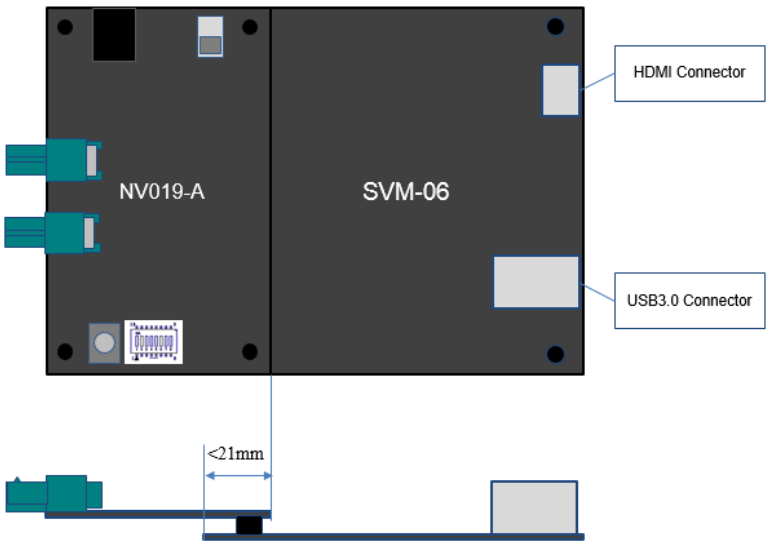


5.2. Drawing

The dimensions of SVM-06 board are shown below. The actual board size does not include the 10mm part to VCUT at each of the top and bottom, and the vertical size is 101.6 [mm] which is the same as our other SV series boards.

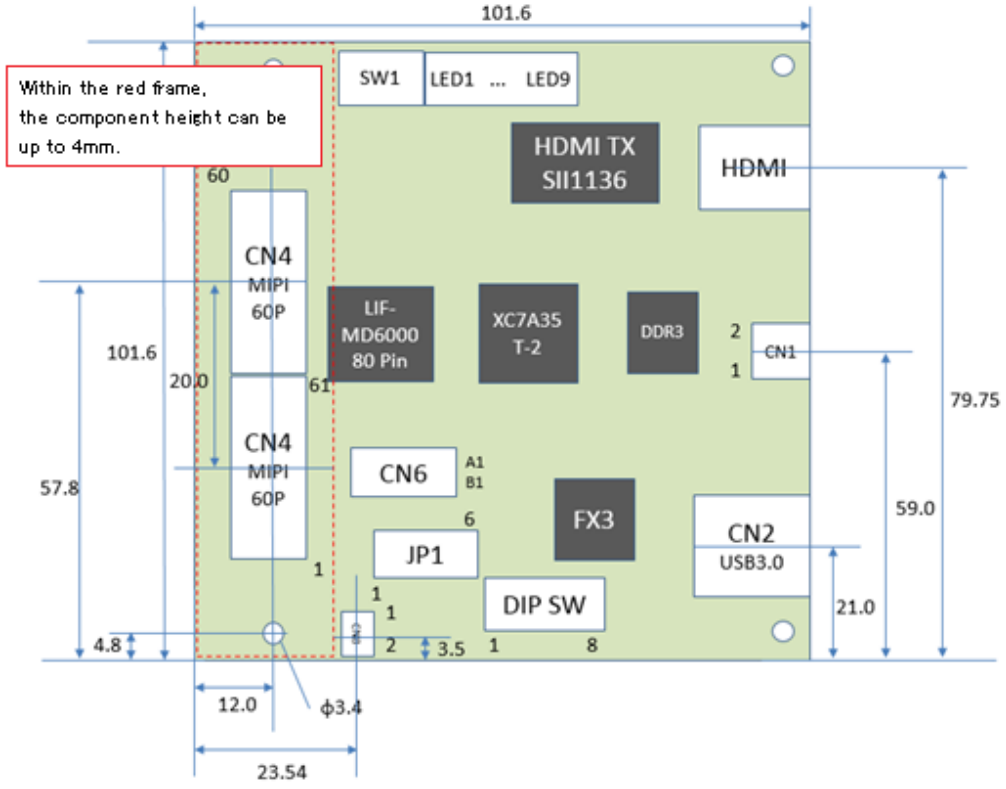


5.3. Dimensional Restriction of Connection Target Board



（Board connection example）

The SVM-06 board is used by connecting the target board to the connector CN4 as shown above. SVM-06. This connection target board is partially overlapped on the SVM-06 board, but the overlapping area of both boards should not exceed 21mm from the board edge of SVM-06. The area where both boards can overlap is indicated by the red frame in the figure below. When using a board to be connected with dimensions that protrude from this frame, pay attention to the board shape, and use high connectors so that both boards can be connected.



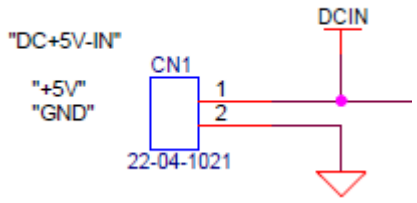
6. Connector Specification

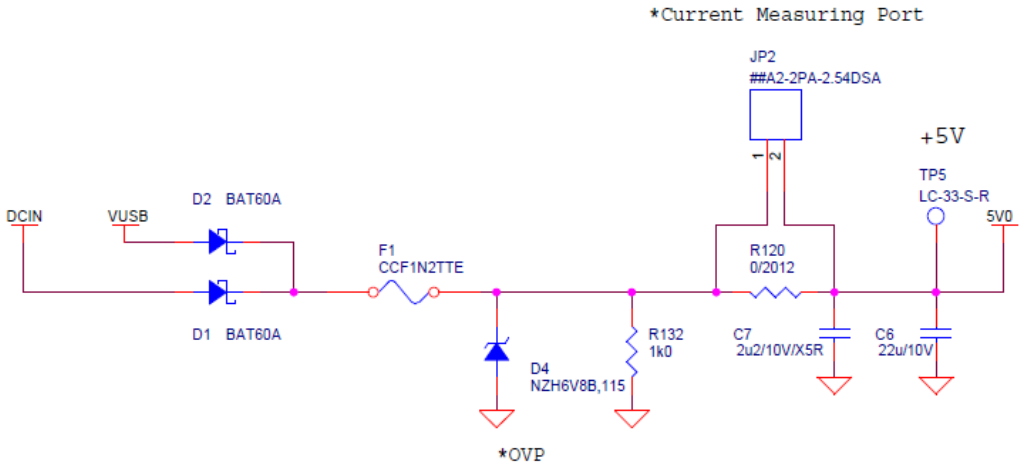
In this chapter, we describe the specifications of the connector used to connect to the image sensor. Other connectors are described in the Appendix.

6.1. CN1: External Power Input Connector

This is used when the power cannot be satisfied by USB bus power or when power is not supplied by USB bus power.

Connector		22-04-1021: Molex					
Pin #	Signal Name	Direction	Remarks	Pin #	Signal Name	Direction	Remarks
1	+5V	IN	DC5V power	2	GND	-	Power ground

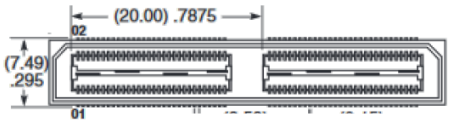




+ 5V (DCIN) from CN1 and + 5V (VUSB) from the USB connector are connected by a diode OR as shown in the above circuit diagram, and are used as a board internal power supply (5V0).

6.2. CN4: Target Connector

This connector is used to connect the target image sensor.



Basic port

Connector		QSH-060-01-L-D-A: SAMTEC					
Pin #	Signal Name	Direction	Description	Pin #	Signal Name	Direction	Description
61	D1_N	IN	MIPI Lane1 Input -	62	GPIO0	IO	GPIO 0 Trigger Signal / FSYNC Signal Input 1
63	D1_P	IN	MIPI Lane1 Input +	64	GPIO1	IO	GPIO 1
65	GND	-		66	GND	-	
67	D3_N	IN	MIPI Lane3 Input -	68	GPIO2	IO	GPIO 2
69	D3_P	IN	MIPI Lane3 Input +	70	GPIO3	IO	GPIO 3 Trigger Signal / FSYNC Signal Input 1
71	GND	-		72	GND	-	
73	CLK_N	IN	MIPI Clock Input -	74	GPIO4	IO	GPIO 4
75	CLK_P	IN	MIPI Clock Input +	76	GPIO5	IO	GPIO 5
77	GND	-		78	GND	-	
79	D2_N	IN	MIPI Lane2 Input -	80	GPIO6	IO	GPIO 6
81	D2_P	IN	MIPI Lane2 Input +	82	GPIO7	IO	GPIO 7
83	GND	-		84	GND	-	
85	D4_N	IN	MIPI Lane4 Input -	86	GPIO8	IO	GPIO 8
87	D4_P	IN	MIPI Lane4 Input +	88	GPIO9	IO	GPIO 9
89	GND	-		90	GND	-	
91	SCL	OUT	I2C SCL Signal Line	92	GPIO10	IO	GPIO 10
93	SDA	IO	I2C SDA Signal Line	94	GPIO11	IO	GPIO 11
95	GND	-		96	GND	-	
97	GND	-		98	GND	-	
99	GND	-		100	GND	-	
101	GND	-		102	GND	-	
103	VSYNC	IN/OUT	VSYNC Input / Output	104	GPIO12	IO	GPIO 12
105	HSYNC	IN/OUT	HSYNC Input / Output	106	GPIO13	IO	GPIO 13
107	GND	-		108	GND	-	

109	CK	OUT	Clock Output (Reserved)	110	GPIO14	IO	GPIO 14
111	RST	OUT	Reset Output (L : Reset)	112	GPIO15	IO	GPIO 15
113	GND	-		114	GND	-	
115	VDDIO	POW	IO Power Output	116	1V2	POW	1.2V Power Output
117	3V3	POW	3.3V Power Output	118	3V3	POW	3.3V Power Output
119	GND	-		120	GND	-	
MP1	GND	-		MP2	GND	-	
MP3	GND	-		MP4	GND	-	

Extension port

Connector		QSH-060-01-L-D-A: SAMTEC					
Pin #	Signal Name	Direction	Description	Pin #	Signal Name	Direction	Description
1	D1_N	IN	MIPI lane5 Input / Output -	2	NC		
3	D1_P	IN	MIPI lane5 Input / Output +	4	NC		
5	GND	-		6	GND	-	
7	D3_N	IN	MIPI lane7 Input / Output -	8	NC		
9	D3_P	IN	MIPI lane7 Input / Output +	10	NC		
11	GND	-		12	GND	-	
13	CLK_N	IN	MIPI clock 2 Input / Output -	14	NC		
15	CLK_P	IN	MIPI clock 2 Input / Output +	16	NC		
17	GND	-		18	GND	-	
19	D2_N	IN	MIPI lane6 Input / Output -	20	NC		
21	D2_P	IN	MIPI lane6 Input / Output +	22	NC		
23	GND	-		24	GND	-	
25	D4_N	IN	MIPI lane8 Input / Output -	26	NC		
27	D4_P	IN	MIPI lane8 Input / Output +	28	NC		
29	GND	-		30	GND	-	
31	SCL	OUT	I2C SCL Signal line	32	NC		
33	SDA	IO	I2C SDA Signal line	34	NC		
35	GND	-		36	GND	-	
37	NC	-		38	GND	-	
39	NC	-		40	GND	-	

41	GND	-		42	GND	-	
43	5V0	POW	+5V Power Output	44	NC		
45	5V0	POW	+5V Power Output	46	NC		
47	GND	-		48	GND	-	
49	NC			50	NC		
51	NC			52	NC		
53	GND	-		54	GND	-	
55	VDDIO	POW	IO Power Output	56	5V0	POW	+5V Power
57	3V3	POW	3.3V Power Output	58	3V3	POW	3.3V Power
59	GND	-		60	GND	-	
MP1	GND	-		MP2	GND	-	
MP3	GND	-		MP4	GND	-	

- The connector position and pin assignment are upward compatible with the 60-pin connector of the conventional board (SVM-MIPI). The interface board for the conventional board can be connected as it is.
- If you do not use the expansion port side (1-60P), you can use it as a 60P connector (connection target: QTH-030-01-L-D-A). In this case, use only the basic port side (61-120P).
- The HSYNC and VSYNC pins are reserved for use for customization. There is no function in the standard version. (Hi-Z)
- GPIO pins are Hi-Z by default. The direction and level of each pin are set by the FPGA register.
- The IO voltage of each single-ended port is determined by jumper JP1.
- The clock output frequency is set with the PC-side utility software "SVMCtl".
- 1.2 V, 3.3 V and 5V can be output about max.150mA.
- SCL and SDA are connected to the I2C bus inside SVM-06 via a level conversion IC.

7. Detail of Each Part

7.1. SW1: Push Switch

SW1 is a switch for reset output and retransmission of register initial settings. Assignment of SW1 function can be changed with SVMCtl.

When you assign SW1 to the reset output, the RST signal line assigned to CN4 is asserted (L output) while SW1 is pressed, and at the same time, the blocks inside the FPGA are reset. When you assign SW1 to the retransmission of register initial settings, it will resend the initialization written to SPI-ROM on board with SVMCtl.

7.2. SW2: DIP Switch

SW2 is 8-bit switch for setting the various modes of operation of SVM-06. You can set the following settings with the switch.

Number	Name	Turns OFF	Turns ON
1	Monitor Output Frame Rate (HDMI Mode Only)	60FPS	30FPS
2	Test Pattern Output	Normal mode	Color Pattern Output
3	Input Lane Setting	The number of input lanes is specified by SW [4:3].	
4	Input Lane Setting	#4=OFF, #3=OFF: 4 Lanes #4=OFF, #3=ON: 1 Lane #4=ON, #3=OFF: 2 Lanes #4=ON, #3=ON: 3 Lanes	
5	Monitor Output Resolution (HDMI Mode Only)	5: OFF, 6: OFF -> 1080p (1920 x 1080) 5: OFF, 6: ON -> 720p (1280 x 720) 5: ON, 6: OFF -> 4k (Only 3840x2160, 30fps) 5: ON, 6: ON -> (Custom resolution) or 1440p (2560x1440)	
6			
7	Working Mode (Effective When Power ON)	7: ON, 8: ON -> (Reserved) 7: ON, 8: OFF -> Start in updater mode 7: OFF, 8: OFF -> Start in HDMI mode 7: OFF, 8: ON -> Start in UVC mode	
8			

- In addition, there is a setting made by the utility software "SVMCtl".
- In HDMI mode, DIP SW # 6 and # 1 settings are valid only when timing data is not set with SVMCtl. If the timing data has been set with SVMCtl, the DIP SW setting is ignored and the video output format set with SVMCtl becomes valid.
- HDMI output is in YUV format at the time of shipment. You can change to RGB format with SVMCtl setting.
- In the "Custom Resolution" setting of the monitor output size setting, when you set the output timing data with SVMCtl, the resolution setting is applied. On the other hand, if you do not set the output timing data, it will be 1440p output.

7.3. LED1-9: Working State Indicator

These LEDs indicate the operating state of the board or FPGA. Flashes rapidly during the startup process. After normal startup, it operates as follows.

LED #	Description
1	Indicates that the power supply to CN4 is valid.
2	Indicates that the clock supplied to the Target is locked.
3	Indicates that Video Sync signal from Target is coming.
4	Turns ON / OFF at the cycle of dividing V-sync from Target by 3.
5	

6	
7	
8	(UVC mode) Indicates that video is being captured from the host PC.
9	(HDMI mode) Turns on / off at the cycle of dividing the V-Sync sync signal to HDMI monitor output by 3. If the output image is 60fps, it will blink 10 times per second. (UVC mode) Turns ON / OFF at the cycle of dividing V-Sync signal to USB output by 3.

7.4. JP1: VDDIO Selection Jumper

JP1 is a jumper for selecting IO power supply (VDDIO) of the target device output from the SVM-06 board to the connector. It can be selected from 1.8 V, 2.5 V, 3.3 V, and can output a current of about 150mA.

VDDIO is intended to be used as an IO supply voltage for image sensors and target devices. And, the GPIO0-15, CLK, RST, SCL, and SDA signal lines are input / output at the VDDIO power supply level.

In default, VDDIO is set to 3.3V.

7.5. JP3: Configuration Setting Jumper

JP3 is a jumper for configuration setting. Normally use it open (no jumper pin connected).

8. Check Terminal

8.1. TP4: VDDIO Check Terminal (red)

TP4 is the check terminal used to check the VDDIO voltage.

8.2. TP1, 3, 5, 6: Voltage Check Terminal (red)

These are the check terminals for each power supply voltage required for the operation of the SVM-06. In normal use, there is no need to check. Besides, do not remove power from these check terminals to supply power to external modules.

8.3. TP7-10: GND Check Terminal (black)

Use it as a GND terminal.

9. Applicable Version

Mode	FX3 Version	FPGA Version
UVC mode	99 or later	1.07 or later
HDMI mode	99 or later	1.07 or later

10. Notes

For proper use of this board, be sure to follow the precautions below.

1. When you update the firmware / FPGA, set the DIP SW (SW2) on the board to # 7 = ON, # 8 = OFF and use the dedicated control software (SVMUpdater) on the host PC.
2. When you connect or take off the target, be sure to turn off the power of the board.
3. we do not guarantee image display on all HDMI monitors about each setting such as output image size and frame rate. Capable of outputting setting is differs from monitors, so nothing may be displayed in the output form that is not supported.
4. Please use a power supply with sufficient current capacity to supply power to this board。Supply power from the personal computer at your own risk. We are not responsible for any damage to your PC.
5. We don't verify 5V power supply to monitor through HDMI cable. Operation is not guaranteed.
6. The contents of this document may be changed without notice.
7. Reprinting all or part of the contents of this document without permission is strictly prohibited.
8. We are committed to the content of this document, but if you find any obscure points, errors, or omissions, please contact us. E-Mail: sv-support@net-vision.co.jp
9. Be sure to use the version or newer SVMCtl / SVMUpdater software provided on the CD-ROM. If you rewrite the SPI-ROM using a previous version of this board, the wrong area may be rewritten.

11. Appendix

11.1. CN2: USB3.0 Connector

CN2 is a USB3.0 connector that connects to the host PC. A commercially available USB3.0 cable can be connected. This connector is also used for power supply of SVM-06.

Connector		USB30B-09K-PC: JC Electronics Corporation					
Pin #	Signal Name	Direction	Description	Pin #	Signal Name	Direction	Description
1	VBUS	IN	+5v Bus Power	2	D-	I/O	USB 2.0 Differential
3	D+	I/O	USB 2.0 Differential	4	GND	-	GND (Power)
5	SSTX-	OUT	USB3.0 Transmission Differential Pair-	6	SSTX+	OUT	USB 3.0 Transmission Differential Pair -
7	GND DRAIN	-	GND (Signal)	8	SSRX-	IN	USB 3.0 Receiver Differential Pair+
9	SSRX+	IN	USB 3.0 Receiver Differential Pair+				

11.2. CN3: HDMI Connector

CN3 is a connector for connecting the HDMI monitor and the like through an HDMI cable.

Connector		5-1903015-1: TE Connectivity					
Pin #	Signal Name	Direction	Description	Pin #	Signal Name	Direction	Description
1	D2+	OUT	TMDS Data 2+	2	D2 shield	OUT	TMDS Data 2 shield
3	D2-	OUT	TMDS Data 2-	4	D1+	OUT	TMDS Data 1+
5	D1 shield	OUT	TMDS Data 1 shield	6	D1-	OUT	TMDS Data 1-
7	D0+	OUT	TMDS Data 0+	8	D0 shield	OUT	TMDS Data 0 shield
9	D0-	OUT	TMDS Data 0-	10	CLK+	OUT	TMDS Clock +
11	CLK shield	OUT	TMDS Clock・shield	12	CLK-	OUT	TMDS Clock -
13	CEC	I/O	CEC Data	14	Utility	IN	Utility
15	DDCSCL	(I)/O	DDC Clock	16	DDCSDA	I/O	DDC Data
17	GND	-	-	18	+5V	OUT	+ 5V Power
19	HPD	IN	Hot Plug Detection				

11.3. CN6: FPGA-JTAG Connector

CN6 is a JTAG port used to write the SPI-ROM of FPGA bitstream or to debug the running FPGA. You don't use it when you use the board normally.

※The direction is seen from the FPGA.

Connector		A3B-14PA-2DSA(71): HRS					
Pin #	Signal Name	Direction	Description	Pin #	Signal Name	Direction	Description
1	GND	-		2	VREF	OUT	Reference Voltage (3.3V)
3	GND	-		4	TMS	IN	JTAG-TMS
5	GND	-		6	TCK	IN	JTAG-TCK
7	GND	-		8	TDO	OUT	JTAG-TDO
9	GND	-		10	TDI	IN	JTAG-TDI
11	GND	-		12	NC	-	Disconnected
13	GND	-		14	NC	-	Disconnected

- **We do not guarantee the operation when you use it.**