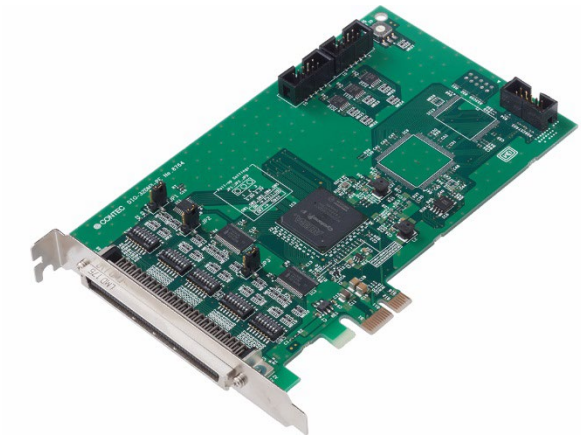
High-Speed Bi-directional
Digital I/O Board for PCI Express

DIO-32DM3-PE



This product is a PCI Express bus-compliant interface board that supports transfer by bus mastering and performs input/output between the external device and digital signal. This product features non-isolated LVTTL level (Operating voltage : 3.3V) I/O 32channels and you can select input / output in 16 units.

Bus master transfer makes it possible to sample quickly large data with transfer rate at 50MHz maximum. It can be used as a pattern generator that outputs arbitrary digital patterns at high speed. It can also be used as a general-purpose I/O board when bus mastering is not used.

Application Software "C-LogicDesigner" is supported. C-LogicDesigner has the pattern generator as well as logic analyzer feature. Windows Linux device driver is also available.

* Specifications, color and design of the products are subject to change without notice.
* The contents in this document are subject to change without notice.
* Visit the CONTEC website to check the latest details in the document.
* The information in the data sheets is as of April, 2026.

Express compatible board DIO-32DM2-PE, DIO-32DM-PE are provided. In addition, as there is compatibility in terms of connector shape and pin assignments, it is easy to migrate from the existing system.

Features

32channels of non-isolated LVTTL level I/O (32 input channels / each 16channels for I/O / 32 output channels are selected.)
This product has the 32channels (operating voltage 3.3VDC, positive logic) of non-isolated LVTTL level I/O whose response speed is 20nsec. They can be used for 32bit input, 16bit input plus 16bit output, or for 32bit output.

Other than I/O bit, this product has the control signal (clock, start, stop and handshake signal (REQ, ACK) that can control starting and stopping the sampling (input) / generating (output)).

Sampling and generating with transfer rate at 50MHz maximum
Bus master transfer makes it possible to sample (input) or generate (output) large data with transfer rate at 50MHz maximum. As the sampling and generating features have their own bus mastering blocks each made up of two independent channels, the board can generate 16 signals while sampling 16 signals.

A synchronization control connector is provided for synchronized control of multiple boards
A synchronization control connector is provided for synchronized control of up to 16 boards. It is also easy to synchronize operation with other CONTEC boards that have a synchronization control connector.

You can use Max. 4 input signals as interrupt request signals at the time of using the general-purpose I/O.
You can use Max. 4 input signals as interrupt request signals and also disable or enable the interrupt in bit units at the time of using the general-purpose I/O.

"C-LogicDesigner" is available.
You can download the application software "C-LogicDesigner" from Contec's website. You can handle the pattern generator as well as the logic analyzer feature without any programming

Windows/Linux support device driver
Using the device driver API-TOOL makes it possible to create applications of Windows/Linux. In addition, a diagnostic program by which the operations of hardware can be checked is provided.

You can use pull-up and the voltage selection
At input points and control signals, you can use pull-up. In addition, the pull-up voltage can be selected from the 3.3V and 5V. This feature allows you to easily connect and equipment with an output point of the sink type.

Functions and connectors are compatible with PCI compatible board PIO-32DM(PCI) and PCI Express compatible board DIO-32DM2-PE, DIO-32DM-PE
The functions same with PCI compatible board PIO-32DM(PCI) and PCI

Packing List

Product...1
Synchronization Control Cable...1
Please read the following...1

Support Software

Name	Contents	How to get
Windows Version Digital I/O Driver software API-DIO(WDM)	The Windows device driver is provided as a form of Windows API functions. Various sample programs such as C# and Visual Basic .NET , Visual C++, Python etc. and diagnostic program useful for checking operation is provided.	Download from the CONTEC website *1
Linux Version Digital I/O Driver software API-DIO(LNX)	The Linux device driver is provided as a shared library. The software includes various sample programs such as gcc (C, C++) and Python programs, as well as a configuration tool to configure the device settings.	Download from the CONTEC website *1
Pattern Generator / Logic Analyzer for Windows C-LogicDesigner	C-LogicDesigner is software that uses a Contec high-speed bidirectional digital I/O device (32DM series) to generate digital signals and provide logic analyzer functions based on sampling.	Download from the CONTEC website *1
Software Development Tool Kits (SDK) and Support Software	In addition to the device drivers, we offer many software programs for using CONTEC devices in an easier manner.	Download from the CONTEC website *2

*1 Download the files from the following URL.
https://www.contec.com/download/
*2 For supported software, search the CONTEC website for this product and view the product page.
https://www.contec.com/

Optional Products

Product Name	Model type	Description
Shielded Cable with Two 96-Pin Half-Pitch Connectors	PCB96PS-0.5P	0.5m
	PCB96PS-1.5P	1.5m
Shielded Cable with One 96-pin Half-Pitch Connector	PCA96PS-0.5P	0.5m
	PCA96PS-1.5P	1.5m
Screw Terminal (M3 * 96)	EPD-96A	*1 *2
Terminal Unit for Relay Terminal Banks	EPD-96	*2
Screw Terminal	DTP-64A	*2

*1 "Spring-up" type terminal is used to prevent terminal screws from falling off.
*2 PCB96PS optional cable is required separately.

Specifications

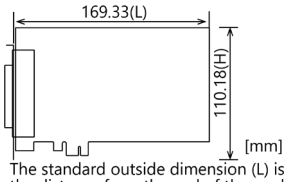
Function specification

Item	Specifications
Digital section	
Number of I/O Channels	32channels (select input 32channels / I/O each 16channels / output 32 channels by software)
I/O circuit	
Operating voltage	3.3VDC
Input section	
Input format	Non-isolated LVTTL level (Equivalent to 74LVT245B) (positive logic) * 5V TTL level input enabled
Pull-up	None/3.3V/5V
Interrupt	<When general-purpose I/O is used> 4 interrupt input signals are arranged into a single output of interrupt signal INTA. An interrupt is generated at the rising edge (LOW-to-HIGH transition).
Pull-up resistor	10kΩ
Output section	
Output format	Non-isolated LVTTL level (Equivalent to 74LVT245B) (positive logic)
Rating (Max.)	3.3VDC 32mA
Response time	20nsec
Data access method	General-purpose digital I/O or I/O with bus master transfer
Echo-back function	Available (at general-purpose output)
Pattern input	
Sampling start trigger	Software start/External start/Pattern match/SC connector
Sampling stop trigger	Software stop/External stop/End of transfer/Transfer error/Specified number of items/SC connector
Sampling clock	Sampling timer/External clock input/handshake/SC connector
Sampling timer	20ns - 21s, 5ns unit
Pattern output	
Generating start trigger	Software start/External start/SC connector
Generating stop trigger	Software stop/External stop/End of transfer/Transfer error/Specified number of items/SC connector
Generating clock	Output timer/External clock input/Handshake/SC connector
Generating timer	20ns - 21s, 5ns unit
Control signal	
I/O signal level	Non-isolated LVTTL level * 5V TTL level input enabled , * 3.3V / 5V pull-up can be set
REQ signal (handshake)	Negative logic tL=25ns (Min.)
ACK signal (handshake)	Negative logic tL=25ns (Min.)
External start signal	Selection of rising/falling edge with the software
External stop signal	Selection of rising/falling edge with the software
External clock input	f=20 MHz (Max.)
Bus master section	
DMA channels	2channels (one each for input and output)
Transfer bus width	64/32bit width
Transfer rate	360 MB/sec.
FIFO	4K data/ch
Scatter/Gather function	2GB/ch
Synchronization section	
Control output signal	Selection of output signal with the software when specifying a sync master board.
Control input signal	Selection of sync factor with the software when specifying sync slave boards.
Max. board count for connection	16 boards including the master board
Common section	
Allowable distance of signal extension	1.5m (dependent on wiring environment)
Memory addresses	Occupies 2 locations 256MByte
Current consumption	3.3V 600mA (Max.) , 12V 30mA (Max.)
Bus specification	PCI Express Base Specification Rev.2.0 x1
Dimension (mm)	169.33(L) x 110.18(H)
Weight	150g

Installation Environment Requirements

Item	Specifications
Operating ambient temperature	0 - 50°C
Operating ambient humidity	10 - 90%RH (No condensation)
Floating dust particles	Not to be excessive
Corrosive gases	None
Standard	VCCI Class A, FCC Class A, CE Marking (EMC Directive Class A, RoHS Directive), UKCA

Physical Dimensions

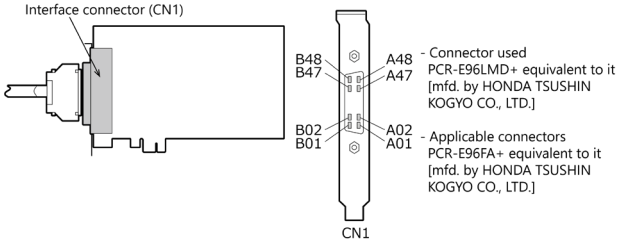


The standard outside dimension (L) is the distance from the end of the card to the outer surface of the slot cover.

Connecting an Interface Connector

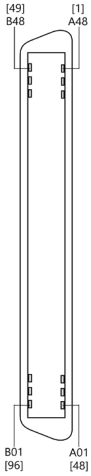
Connecting an Interface Connector

To connect an external device to this product, plug the cable from the device into the interface connector (CN1) shown below.



Layout on the Interface Connector(CNA, CNB)

GND	B48		A48	GND
GND	B47		A47	GND
GND	B46		A46	GND
EXTCLK1	B45		A45	EXTCLK0
GND	B44		A44	GND
EXTSTART1	B43		A43	EXTSTART0
GND	B42		A42	GND
EXTSTOP1	B41		A41	EXTSTOP0
GND	B40		A40	GND
EXTREQ1	B39		A39	EXTREQ0
GND	B38		A38	GND
EXTACK1	B37		A37	EXTACK0
GND	B36		A36	GND
GND	B35		A35	GND
GND	B34		A34	GND
DIOD07	B33		A33	DIOB07
GND	B32		A32	GND
DIOD06	B31		A31	DIOB06
GND	B30		A30	GND
DIOD05	B29		A29	DIOB05
GND	B28		A28	GND
DIOD04	B27		A27	DIOB04
GND	B26		A26	GND
DIOD03	B25		A25	DIOB03
GND	B24		A24	GND
DIOD02	B23		A23	DIOB02
GND	B22		A22	GND
DIOD01	B21		A21	DIOB01
GND	B20		A20	GND
DIOD00	B19		A19	DIOB00
GND	B18		A18	GND
DIOC07	B17		A17	DIOA07
GND	B16		A16	GND
DIOC06	B15		A15	DIOA06
GND	B14		A14	GND
DIOC05	B13		A13	DIOA05
GND	B12		A12	GND
DIOC04	B11		A11	DIOA04
GND	B10		A10	GND
DIOC03	B09		A09	DIOA03 *1
GND	B08		A08	GND
DIOC02	B07		A07	DIOA02 *1
GND	B06		A06	GND
DIOC01	B05		A05	DIOA01 *1
GND	B04		A04	GND
DIOC00	B03		A03	DIOA00 *1
N.C.	B02		A02	N.C.
N.C.	B01		A01	N.C.



[ ] shows the pin No. of HONDA TSUSHIN KOGYO CO., LTD. specification.

*1 Can be used as an interrupt signal when used as general-purpose I/O.

Signal name	Description
DIOA00 - DIOA07	I/O signal DIOA00 - DIOA07 DIOA00 - DIOA03 can be used as interrupt signal DIOIn00 - DIOIn03 at the time of general-purpose I/O.
DIOB00 - DIOB07	I/O signal DIOB00 - DIOB07
DIOC00 - DIOC07	I/O signal DIOC00 - DIOC07
DIOD00 - DIOD07	I/O signal DIOD00 - DIOD07
EXTCLK0 - EXTCLK1	External clock input
EXTSTART0 - EXTSTART1	External start signal
EXTSTOP0 - EXTSTOP1	External stop signal
EXTREQ0 - EXTREQ1	REQ signal
EXTACK0 - EXTACK1	ACK signal
GND	This is connected to GND of slot.
N.C.	This pin is left unconnected.

Connection method to the external device -Data I/O-

Connecting the data I/O signal(DIOA0* - DIOD0*)

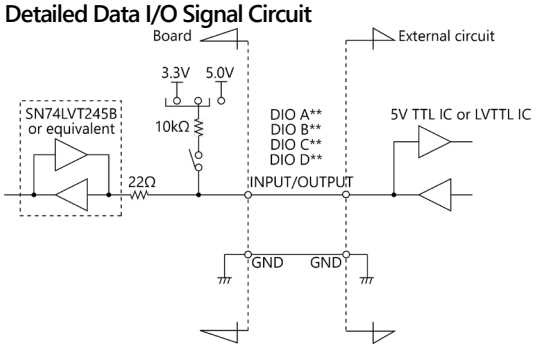
These lines input from and output to external devices and can be configured in 16bit with the software.

Input and output and setting procedures are the same whether these lines are used for general-purpose digital I/O or bus master transferring and they can be configured in three different settings as shown below:

Signal name	Setup1	Setup2	Setup3
DIOA00 - DIOA07	Input	Input	Output
DIOB00 - DIOB07	Input	Input	Output
DIOC00 - DIOC07	Input	Output	Output
DIOD00 - DIOD07	Input	Output	Output

When settings 1 and 2 are used for general-purpose digital I/O, DIOA00 through DIOA03 can be used as interrupts (rising edge).

Detailed Data I/O Signal Circuit



Connection method to the external device -Control I/O-

Connection to the control signal (EXT**)

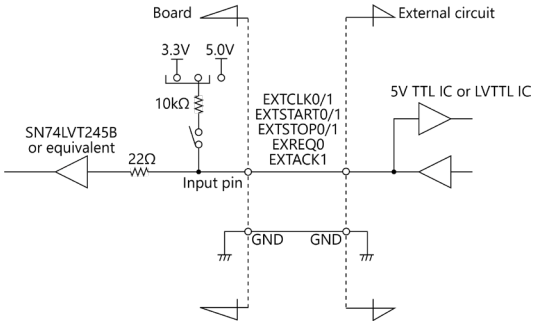
In order to control bus mastering from outside, five signals are provided each for pattern I/O. Before using the signals to be input as control signals please verify their pulse widths.

"0" at the end of a signal name indicates a pattern input signal and "1" a pattern output signal.

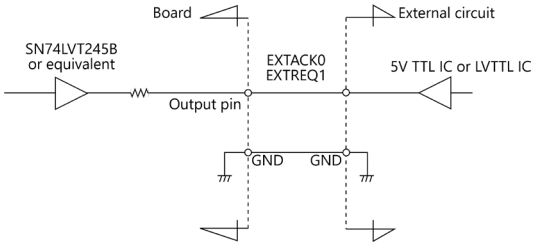
Signal name	Direction	Usage	Signal name	Direction	Usage
EXTCLK0	In	Pattern input clock	EXTCLK1	In	Pattern output clock
EXTSTART0	In	Pattern input start signal	EXTSTART1	In	Pattern output start signal
EXTSTOP0	In	Pattern input stop signal	EXTSTOP1	In	Pattern output stop signal
EXTREQ0	In	Pattern input REQ signal	EXTREQ1	Out	Pattern output REQ signal
EXTACK0	Out	Pattern input ACK signal	EXTACK1	In	Pattern output ACK signal

Detailed Control Input Signal Circuit

Control signals to be input include clock, start, stop, and handshake input signals.



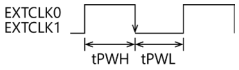
Detailed Control Output Signal Circuit



What is the Control Signal ?

- External clock signal (EXTCLK0/EXTCLK1)

These signals input external pacer clocks. The maximum frequency is 20MHz. When the external clock input is set as the clock source, pattern input or output occurs at the falling edge of this signal.

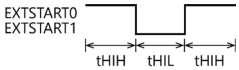


tPWH : Clock pulse high width 25ns (Min.)

tPWL : Clock pulse low width 25ns (Min.)

- Eternal start signal (EXTSTART0/EXTSTART1)

These input signals start bus mastering with an external signal. The signal level is LVTTL and you can select and enable the rising or falling edge with the software. In order to detect the signal edge, a high- and low-level hold time of 25ns is needed at minimum.



tHIH : High level hold time 25ns (Min.)

tHIL : Low level hold time 25ns (Min.)

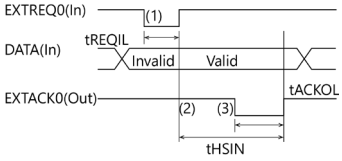
- External stop signal (EXTSTOP0/EXTSTOP1)

These input signals stop bus mastering with an external signal. The signal is LVTTL level and you can select and enable the rising or falling edge with the software. In order to detect the signal edge, a high- and low-level hold time of 50ns is needed at minimum.

- Handshake Signal (EXTREQ0/EXTACK0/EXTREQ1/EXTACK1)

These signals handshake with external devices. The signal is LVTTL level and controlled with negative logic.

Handshake Signals at the Time of Input



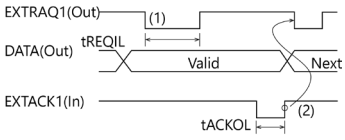
tREQIL : EXTREQ0 low width 25ns (Min.)

tACKOL : EXTACK0 low width 100ns

tHSIN : Handshaking time 100ns (Min.)

1 After setting the handshaking operation, this product samples the EXTREQ0 signal and starts pattern input when it recognizes a low pulse of more than 25ns. Pattern data prior to that time is disabled.
2 The board generates a cycle to write data input from an external device to the PC memory by bus mastering.
3 At the end of writing data, the board outputs acknowledge signal EXTRACK0 to notify the external device.

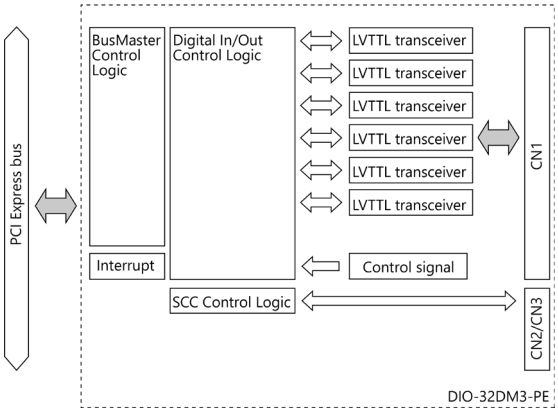
Handshake Signals at the Time of Output



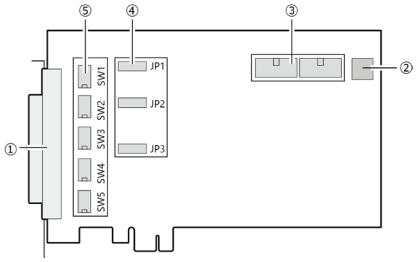
tREQOL : EXTREQ1 low width 100ns
tACKOL : EXTACK1 low width 25ns (Min.)

1 After setting the handshaking operation, this product outputs the EXTREQ1 signal.
2 The board begins sampling acknowledge signals from external devices. The board recognizes the end with a low pulse of more than 25ns and, at the leading edge, starts preparing to output the next data.

Block Diagram



Nomenclature of Product Components



No.	Name	No.	Name
1	Interface Connector	4	Pull-up voltage setting jumper
2	Board ID Setting Switch	5	Pull-up voltage setting switch
3	Synchronous control connectors		

Differences between DIO-32DM3-PE, DIO-32DM2-PE, DIO-32DM-PE and PIO-32DM(PCI)

Differences between DIO-32DM3-PE and PIO-32DM(PCI)

	DIO-32DM3-PE	PIO-32DM(PCI)
Input format	Non-isolated LVTTL level (Equivalent to 74LVT245B) (positive logic) * 5V TTL level input enabled	Non-isolated TTL level (Equivalent to 74ALS245A) (positive logic)
Pull-up	None/3.3V/5V	5V
Output format	Non-isolated LVTTL level (Equivalent to 74LVT245B) (positive logic)	Non-isolated TTL level (Equivalent to 74ALS245A) (positive logic)
Response time	20nsec	50nsec
Control signal	Non-isolated LVTTL level (Equivalent to 74LVT245B) Non-isolated LVTTL level (Equivalent to 74LV125A) * 5V TTL-level input enabled * 3.3V / 5V pull-up can be set	Non-isolated TTL level (Equivalent to 74ALS245A) Non-isolated TTL level (Equivalent to 74LS125A)
Bus specification	PCI Express Base Specification Rev.2.0 x1	PCI(32bit, 33MHz, Universal key shapes supported)
Input format	3.3V 600mA (Max.) , 12V 30mA (Max.)	5V 700mA (Max.)

Differences between DIO-32DM3-PE, DIO-32DM2-PE and DIO-32DM-PE

	DIO-32DM3-PE	DIO-32DM2-PE	DIO-32DM-PE
Input format	Non-isolated LVTTL level (Equivalent to 74LVT245B) (positive logic) * 5V TTL level input enabled	Non-isolated LVTTL level (Equivalent to 74LV245A) (positive logic) * 5V TTL level input enabled	Non-isolated LVTTL level (Equivalent to 74LV245A) (positive logic) * 5V TTL level input enabled
Pull-up	None/3.3V/5V	None/3.3V/5V	None
Output format	Non-isolated LVTTL level (Equivalent to 74LVT245B) (positive logic)	Non-isolated LVTTL level (Equivalent to 74LV245A) (positive logic)	Non-isolated LVTTL level (Equivalent to 74LV245A) (positive logic)
Response time	20nsec	50nsec	50nsec
Control signal	Non-isolated LVTTL level (Equivalent to 74LVT245B) Non-isolated LVTTL level (Equivalent to 74LV125A) * 5V TTL-level input enabled * 3.3V / 5V pull-up can be set	Non-isolated LVTTL level (Equivalent to 74LV245A) Non-isolated LVTTL level (Equivalent to 74LV125A) * 5V TTL-level input enabled * 3.3V / 5V pull-up can be set	Non-isolated LVTTL level (Equivalent to 74LV245A) Non-isolated LVTTL level (Equivalent to 74LV125A) * 5V TTL-level input enabled
Bus specification	PCI Express Base Specification Rev.2.0 x1	PCI Express Base Specification Rev.1.0a x1	PCI Express Base Specification Rev.1.0a x1
Operating voltage	3.3V 600mA (Max.), 12V 30mA (Max.)	3.3V 400mA (Max.), 12V 30mA (Max.)	3.3V 400mA (Max.)